USBPGF-S1

The USBPGF-S1 USB Controlled Precision Software Configurable Instrumentation Amplifier Low Pass Filter System

USBPBP-S1

The USBPBP-S1 USB Controlled Precision Software Configurable Instrumentation Amplifier Band Pass Filter System

USBPHP-S1

The USBPBP-S1 USB Controlled Precision Software Configurable Instrumentation Amplifier High Pass Filter System

USBPIA-S1

The USBPIA-S1 USB Controlled Precision Software Configurable Instrumentation Amplifier System

USBDR-8

The USBDR-8 8-channel USB and power distribution rack

Guide to Operations

Part Numbr 400016
Revision F

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Cautions and Warnings

 Software drivers for the USBPxx-S1 must be installed prior to connecting the USB cable to the target computer.

 The USBPxx-S1 contains static sensitive devices.

Declaration of Conformity

We declare under sole responsibility that the USBPxx-S1 meets the essential health and safety requirements and are in conformity with the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents.

EC Directive 89/336/EMC: 1989

Essential health and safety requirements relating to electromagnetic compatibility.

EN50081-1 Class B

Generic emissions standard for residential, commercial, and light industrial products (Limits and methods of measurements of electromagnetic disturbance characteristics of industrial, scientific, and medical (ISM) radio frequency equipment).

EN55022 – Radiated emissions and power line conductions
EN50082-1 – Generic immunity standards for residential, commercial, and light industrial products
EN61000-4-2 (IEC801-2) – Electrostatic discharge
EN61000-4-3 (IEC801-3) – RF immunity
EN61000-4-4 (IEC801-4) – Electrical fast transients

1 Overview

Figure 1-1 The USBPGF-S1

This guide to operations covers both the USBPGF-S1, USBPBP-S1, USBPHP-S1, and the USBPIA-S1. In function, the USBPIA-S1, USBPGF-S1, and USBPHP-S1 are subsets of the USBPBP-S1. When features are shared between the models, the model is referenced by the name "USBPxx-S1" if the feature is exclusive to the USBPGF-S1 then it is referenced by the name "USBPGF-S1". The USBPxx-S1 is a stand-alone USB controllable module that provides a single channel of low-pass filtering and or high-pass filtering (USBPGF-S1 low pass only) (USBPHP-S1 high pass only) and or high-quality instrumentation amplifier (USBPIA instrumentation amplifier only), optional AC coupling (USBPGF-S1 and USBPIA-S1 only), for front-end signal conditioning compatible with all popular A/D converter devices.

The USBPxx-S1 is powered with 9 to 12VDC so it can be connected to a battery voltage source or the supplied 115-220VAC adapter may be used for operation with wall power anywhere in the world. The plugs on the supplied VAC adapter are detachable and interchangeable. The appropriate plug is delivered to the destination country to be compatible with the local wall power outlet. If the USBPxx-S1 is to be used in a location different from the initial destination country then additional wall power adapter plug modules may be purchased. Please visit our web site http://www.alligatortech.com for USBPxx-S1 accessory purchase details.

When programmed from the USB port, the USBPxx-S1 will remember all of the programmed properties between power cycles. Program once and operate as a stand- alone signal conditioner without having to reprogram for every use. This is perfect for turn-key applications. Unauthorized people, therefore those with no access to the Windows control software, cannot change the parameters of the USBPxx-S1.

It's easy to connect the USBPxx-S1 into the data collection system. Input and output signals can be routed through BNC connection or using the detachable screw terminal connectors. Optional SMA type adapters are also available. Additional screw terminal connector adapters may be purchased. Please visit our web site http://www.alligatortech.com for USBPxx-S1 accessory purchase details.

1.1 Match the filter characteristics to best suit the application

Each USBPxx-S1 is factory configured with a wide choice of filter characteristics. Choose from Butterworth, Bessel, elliptic(Cauer), or linear phase filters. High stop-band attenuation of -90dB is available. The USBPxx-S1 Instrumentation Amplifier provides an excellent common-mode rejection of 90 to 100 dB typical at high gains. Please visit our web site http://www.alligatortech.com for a tutorial on filter characteristic selection.

1.2 Protection from high input voltages

The USBPxx-S1 will pass a signal voltage within the range of +/-10V. The USBPxx-S1 provides strong input protection and can withstand up to +/-40V at the analog signal input.

1.3 Amplify and then filter to improve the signal to noise ratio

The USBPxx-S1 high-quality instrumentation amplifier provides software-selectable gain as well as differential inputs with high-common mode rejection. Gain can be set at 1, 2, 5, 10, 20, 50, 100, 200, 500 or 1000. Most A/D devices provide a gain amplifier stage. For applications where the target signal is imbedded in high voltage noise, the USBPGF-S1 gain can be set to 1 to filter the signal first and then amplify with the A/D converter gain. For all other applications it is recommended to amplify small voltage input signals before filtering to maximize the signal to noise ratio of the sampled signal. The USBPHP-S1 and the USBPBP-S1 high pass filter sections are located before the programmable amplifier to remove low oscillations or DC offset before amplification of the signal.

1.4 Single-Ended or Differential input connection

The signal source can be connected to the USBPxx-S1 input either single-ended or differentially. The input BNC connector is a differential input connecting the inner pin receptacle to the instrumentation amplifier signal high and the outer ring to signal low. For single-ended input applications the signal source ground at the BNC can be connected to the USBPxx-S1 analog ground by using a wire shunt on the input screw terminal connector. No software configuration is necessary to select the single-ended differential modes. The use of either mode is dependent on how the connections are made. Connections can be made using either the BNC input connector or the screw terminal connector.

1.5 Software select any corner frequency

The corner frequency of each low pass filter on the USBPBP-S1 and USBPGF-S1 is software controlled to select any corner frequency from 0.1Hz to the maximum frequency of each factory installed filter characteristic. Control the Butterworth filter up to 100kHz. Control the Bessel filter up to 66kHz. Control the Elliptic filter up to 50kHz and the high frequency Elliptic to 100kHz. Control the Linear Phase filter up to 200kHz. Each USBPxx-S1 in a multi-channel data collection system can have a unique filter characteristic, a unique corner frequency, and a unique amplification. Optionally, an external clock signal can be used to control the corner frequency in tracking filter applications.

For the USBPBP-S1 and USBPHP-S1 the high pass filter section are available as a 4-pole Butterworth or Bessel characteristic and can be software controlled to select any corner frequency within a range of frequencies. Both filter characteristics are available as the standard selectable corner frequency range from 5Hz to 1027Hz. When configured with the extended range factory option the selectable corner frequency range extends from 184Hz to 44.77kHz. When using the USBPBP-S1 it should be noted that if the high pass filter corner frequency is set to a higher frequency then the low pass filter corner frequency and the rejection bands of each filter overlap, all frequencies in the signal will be rejected across entire frequency band.

1.6 AC couple at any time

The USBPGF-S1 and USBPIA-S1 can AC couple or DC couple the input signal under software control. This feature is useful in applications where the input signal is coupled to a large DC offset. AC coupling will remove the DC offset.

1.7 All Software is Included

The USBPxx-S1 comes with a complete menu-driven program.

SystemViewUSBPxx is a ready-made Windows NT,XP,Vista,7 compatible application that uses a few simple mouse clicks to program the parameters of each USBPxx-S1 connected to the PC. Once selected, the desired parameters are set and saved to non-volatile memory in the USBPxx-S1 so that they are reapplied after every subsequent power up.

1.8 DC Offset continuously compensated

The low pass filter section in the USBPGF-S1 and USBPBP-S1 features automatic electronic DC offset compensation and is highly suited in applications requiring minimal offset from the sampling system. The DC offset specification is listed with the DC offset compensation enabled. The DC offset compensation circuitry may be optionally disabled at the factory.

The DC offset specification reflects the actual electronic operation and does not require extra software normalization techniques using stored constants.

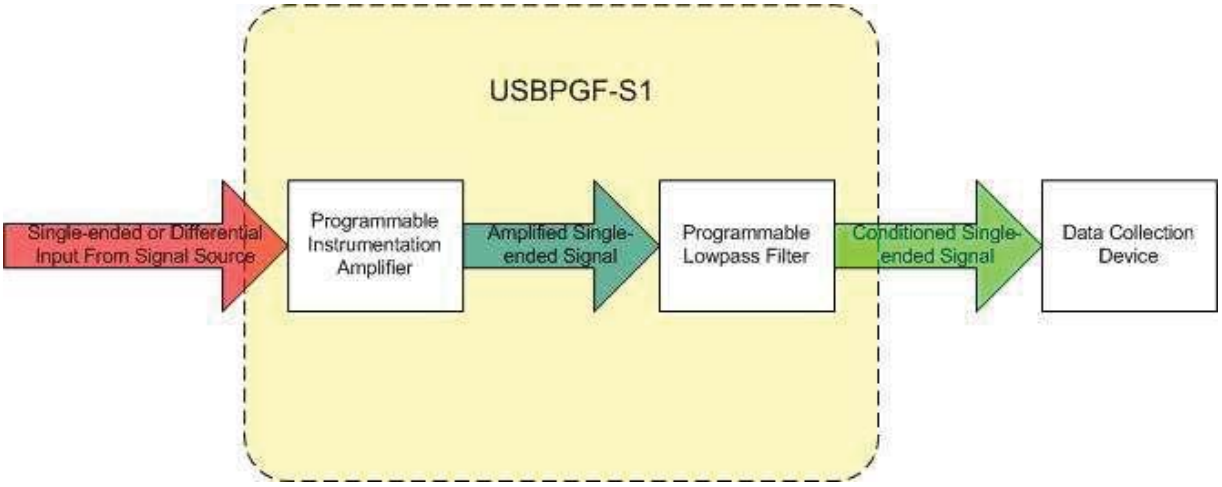


Figure 1-2 The Analog Signal Path

2 Setup and Installation

 Software drivers for the USBPxx-S1 must be installed prior to connecting the USBPxx-S1 into the target computer.

 The USBPxx-S1 contains static sensitive devices. Disassembly of the protective enclosure will void the warranty.

2.1 Install the SystemViewUSBPxx software

To start the software installation, place the SystemViewUSBPxx installation software in a temporary subdirectory and run **SETUP.EXE**. Follow the instructions on each of the displayed steps and then press **Next** to continue to the next step. To complete the installation process press **Finish**. Once the installation process is complete, the USBPxx-S1 can be connected with the provided USB cable to the host computer.

2.2 The USB Device Driver Installation

When the USBPxx-S1 is connected to the host computer, the Windows operating system will recognize the device and automatically load the correct USB device driver. A message may appear near the system icon tray acknowledging device recognition that the device is ready to use. If the USBPxx-S1 is not recognized, make sure the connections are secure and the USBPxx-S1 is powered. Try re-installing the software if the situation persists.

2.2.1 Uninstalling the software

If it becomes necessary to uninstall the existing USBPxx-S1 support software, this can be done through the **Windows Control Panel – Add and remove programs** utility. Scroll down the list of displayed programs and find **SystemViewUSBPxx** and select **remove**. Follow the instructions on the screen to proceed through the uninstall steps.

2.3 Hardware Installation

 Make all analog signal path connections with the power disconnected. Connecting the analog signals with the power connected can introduce spurious voltages beyond the safety limits of the USBPxx-S1 and can damage the internal components. Damage caused in this manner is not covered by the warranty.

Power can be applied to the USBPxx-S1 before or after connecting the USB to the host computer.

Figure 2-1 Connecting Power to the USBPxx-S1

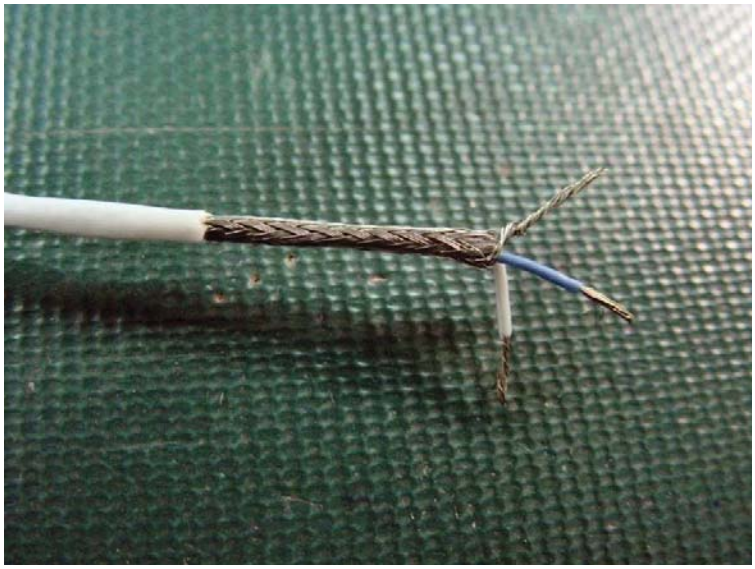
The USB connector on the USBPxx-S1 is type B. The provided cable is a standard 1M length type A USB to type B USB. Additional cables can be purchased. Please visit the web site http://www.alligatortech.com for details. Once the software has been installed, the USBPxx-S1 can be connected to the USB port of the PC before or after starting SystemViewUSBPxx. Multiple USBPxx-S1 units can be connected to the same PC at the same time. There is virtually no logical limit to the number of USBPxx-S1 devices that can be connected simultaneously. The SystemViewUSBPxx software will recognize each device as an individual unit and any of the simultaneously connected devices can be communicated to at any time without limitation. The USBPxx-S1 does not use power supplied through the USB port therefore the physical limitation of the number of devices that can be simultaneously connected through each USB port is the number allowed by the USB port manufacturer. Multi-port USB hubs may be used to increase access to the main USB port. Some computers are supplied with multiple USB ports. Each port can support the maximum number of devices. Typically, one computer can support the simultaneous connection of over 1000 USB devices. The USBPxx-S1 will not interfere with the function of any other device connected to the same main USB port.

Figure 2 2 Connecting USB to the USBPxx-S1

3 Connection To A/D Devices and Signal Sources

3.1 I/O Cabling

The analog signal path cables are the most likely source for failure and signal degradation in the sampling system. Save time and money and use high quality cables. The BNC connectors are supplied for convenience however, it is not recommended to use coaxial cable for connections of lengths longer than 0.25 meters. This is because parallel wires, the outer shell and the inner wire, are susceptible to capacitive coupling and the introduction of common mode noise into the signal path. The longer the wire length used, the higher the susceptibility to problems will exist.



igure 3-1 High Quality Cable

3.1.1 Connect Signal Source to the USBPxx-S1 Input

If the signal source is over 0.5M from the USBPxx-S1 input, it is strongly recommended to make input connections differentially.

3.1.1.1 Differential Connections

From the signal source to the USBPxx-S1 input, whenever possible, use cable that has two twisted wires and an outer shield encasing the twisted wires. Use one wire for signal high where current flows towards the USBPxx-S1 input and connect this wire to **In Hi**. Use the second wire for signal low where the current flows away from the USBPxx-S1 and connect this wire to **In Lo**. The shield is used to connect the signal source ground to the USBPxx-S1 ground, **A Gnd**. It is a preferred configuration to connect the signal ground connection to the USBPxx-S1 ground however it is optional in some applications.

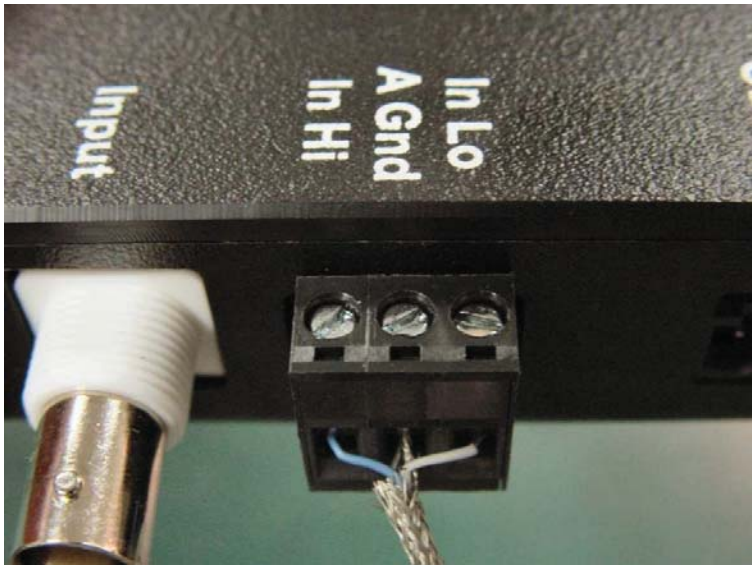


Figure 3-2 Differential Input Connection

3.1.1.2 Single-ended Connections

When using the BNC connector for single-ended input it is recommended to connect the USBPxx-S1 **A Gnd** to **In Lo** using very short wire as shown in the picture below. This is because the BNC input connector is wired for differential use meaning that without the wire shunt, **In Lo** would be attached to the ground of the signal source but not to the ground of the USBPxx-S1.

Figure 3-3 Single-ended connection with BNC and wire shunt

It is also recommended to use the wire shunt when using the screw terminal connector for single-ended connections. In all cases, it would be improper to leave **In Lo** unconnected to the signal source. The open **In Lo** will float and **In Hi** will be referenced to a floating signal leading to grossly erroneous results.

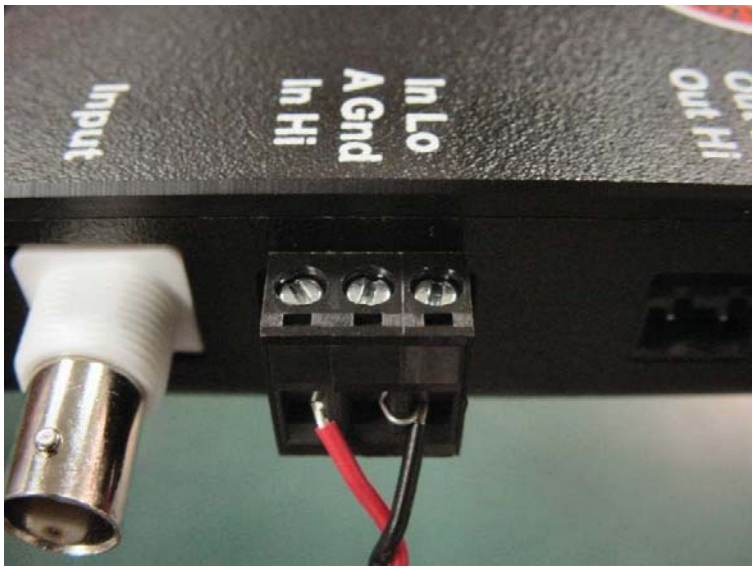


Figure 3-4 Single-ended connection with ground shunt

3.1.2 Connect USBPxx-S1 Output to the A/D Device

The USBPxx-S1 output is single-ended only. Therefore it is imperative to use very short lengths

of high quality cable from the USBPxx-S1 to the A/D input.

3.1.3 By-passing the filter

All by-passing must be done external to the USBPxx-S1. The input screw terminal connector can be used as a junction point for by-passing. Do not leave the output of the USBPxx-S1 connected to the by-passed signal.

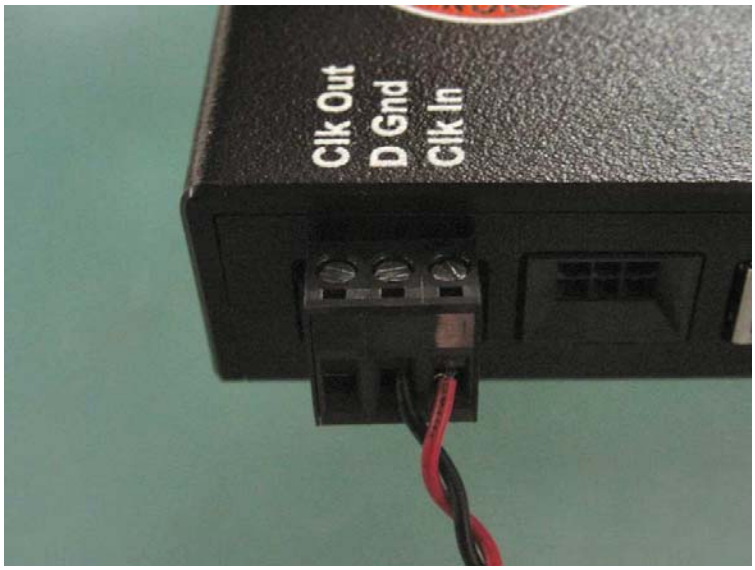
3.2 Internal and External Filter Clock Signals

In most applications the internally generated filter clock source is sufficient for controlling the USBPGF-S1 and USBPBP-S1 low pass filter corner frequencies and use of the external clock input is not necessary. If external filter clock control of the corner low pass corner frequency is required, the external clock signal must be wired to **Clk In** with its return to the **D Gnd** (digital ground) pin. The external clock input is enabled in software.

PLEASE TAKE NOTE: if there is no clock supplied and the external clock input is enabled, the low pass filter in the USBPGF-S1 and USBPBP-S1 will not operate. The output of the filter will drift quickly to the positive or negative power rail. This will saturate the DC offset compensation circuit. When a clock is restored, it will take approximately 90 seconds for the DC offset compensator to recover. We strongly recommend purchasing the USBPGF-S1 and USBPBP-S1 with the DC offset compensation disabled for applications requiring external clock control where the presence of an external clock cannot be guaranteed and the recovery period is not acceptable.

Some reasons for using an external clock are:

- The frequency must be changed faster than software can access the board.
- The frequency must track some other waveform such as a tracking filter.
- Synchronization of the A/D conversion cycle.



3-5 Connecting an external clock to the USBPGF-S1

The external clock source must be set at the frequency calculated from the filter type constant multiplied by the desired corner frequency. Please refer to the table of constants below.

Product Designation	Filter Characteristic	Ratio Fclock:Fcorner (Hz)
USBPGF-S1/B	Butterworth	50:1
USBPGF-S1/L	Bessel	75:1
USBPGF-S1/CE	Cauer-Elliptic	100:1
USBPGF-S1/HC	High Bandwidth Cauer-Elliptic	50:1
USBPGF-S1/LP	Linear Phase	50:1
USBPGF-S1/HLP	High Bandwidth Cauer-Elliptic	25:1

Table 3-1 Filter clock to corner frequency (Fc) ratio

The filter clock must be a TTL- or CMOS-logic-level square wave with symmetry, duty cycle, of 50% ±10%. A less symmetric waveform may increase the output noise level of the filter. The frequency of the clock must be set between 10 Hz and 5 MHz. If the driver is TTL, a pull-up resistor to +5 volts will improve the voltage margins. The filter corner frequency will be a fraction of the clock frequency.

3.2.1 External Clock Waveform Specifications

Nominal electrical characteristics	+5V CMOS (or good TTL) square wave
Frequency	10 Hz to 5 MHz (7MHz for Bessel or Butterworth)
Low level	+0.8V
High level	+2.8V
Duty cycle	50% is preferred, but any waveform with high and low intervals each at least as long as a square wave at maximum clock frequency (i.e., each 100ns for the standard model) will work
Maximum rise and fall times	10% or 1 microsecond, whichever is less
Load	CMOS input

3.2.2 Clk Out

Clk Out, is used in applications requiring A/D synchronization to the USBPGF-S1 or USBPBP-S1 internal filter clock. It will be discussed elsewhere in this guide.

Due to the sharp rise and fall edges of the clock signals, they can radiate considerable EMI from the cables. Shielded wires, with the shield forming the DGND connection at both ends, are preferred for them. At least, the DGND wire must be physically adjacent to the clock wire, preferably twisted with it.

3-6 Connecting Pacer Clock Output

3.3 Grounding

Six types of ground references complicate the setup of an instrumentation system: earth, chassis, DC power, digital, analog or A/D converter, and measured-signal.

- **Earth ground or AC Ground** – The ground reference for the AC mains. It connects to the third pin on an AC-power wall plug.

  Earth ground is designed to prevent electrical shocks and ultimately connects to such true grounds as a water pipe.

- **Chassis Ground** - The metal structure or case of an electronic system. For safety reasons, chassis ground must be connected to the earth-ground pin of the wall plug. When the case of the measurement system is attached to this pin, the event of a short

circuit between the “hot” power line and the metal case will trip the main power circuit breaker or the power fuse instead of electrocuting someone who has become part of the circuit.

- **Digital (Power) Ground** - This is the common return point for digital signals. In most instrumentation systems, the logic "0" digital signal level will be at or near this level, while the "1" will be a few volts higher.

  Unlike earth and chassis ground, digital ground often carries signals with high-frequency components. To provide a low-inductance return path for such currents, digital ground lines must be run close to the signal lines. If a digital signal is sent over a shielded wire, the shield must be connected to digital ground.

  In many systems, digital ground is connected to DC power ground, allowing it to be used as a DC power ground for non-critical circuits.

- **DC Power Ground** - The common return point for the DC power supplies. DC power ground, which is often connected to chassis ground, includes the "ground" pins on the PC bus connected to the power ground.

- **Analog Ground or A/D Converter Ground** - The common return point for critical analog signals. Wires connected to this point should not be allowed to carry appreciable DC, AC, or high-frequency components. If they do, the resistive or inductive voltage drops could cause measurement errors.

  In a single-ended measurement system, analog ground serves as the reference point against which signal voltages are measured. In a differential system, analog ground is the point against which common-mode voltages are measured.

  Being able to operate circuits like A/D converters that have both digital and analog elements means a reference analog ground must be connected to digital or DC power ground. This connection often is made within the A/D board circuits. This should be the only place where analog ground and digital ground are connected together.

- **Measured-Signal Ground** - The common return point of the signal sources, including the transducer and other controls. If all measurements are differential, measured-signal ground need not exist, although signal returns can still be connected in common for convenience, and there can be an overall "grounded" shield.

  When it does exist in a differential system, measured-signal ground frequently is connected to analog ground. However, it need not be connected to anything as long as the system has sufficient common-mode voltage range and common-mode rejection.

  If any measurements are single-ended, measured-signal ground must exist and it must be connected to analog or A/D ground.

4 Software Operation

4.1 Overview

In all new installations, install the low level libraries by selecting Setup.exe from the downloaded web distribution. The setup program will also install SystemViewUSBPxx. SystemViewUSBPxx should be used to verify the proper operation of the USBPxx-S1 even if it is ultimately intended to use custom developed control software. This will insure that the product and low level device drivers have been installed properly and do not encounter interference with other hardware in the data collection system. The best method to test the installation is to provide a known test signal, preferably a sine wave, generated by a signal generator and monitored at the output by an oscilloscope or the intended A/D device. Use the software controls to change the function of the product and observe the output for the expected result.

SystemViewUSBPxx is a dialog window program that controls the AC couple, gain, clock source, filter corner frequency, and the external clock output of all USBPxx-S1 devices connected to the host system. It displays two types control screens, which contain a similar appearance for selecting these parameters. The centered SystemViewUSBPxx main screen can be used for globally controlling all of the USBPxx-S1 devices simultaneously connected with common parameters. A specific USBPxx-S1 dialog window cascaded from the upper left of the screen, can be used to control a unique set of parameters on a specific device.

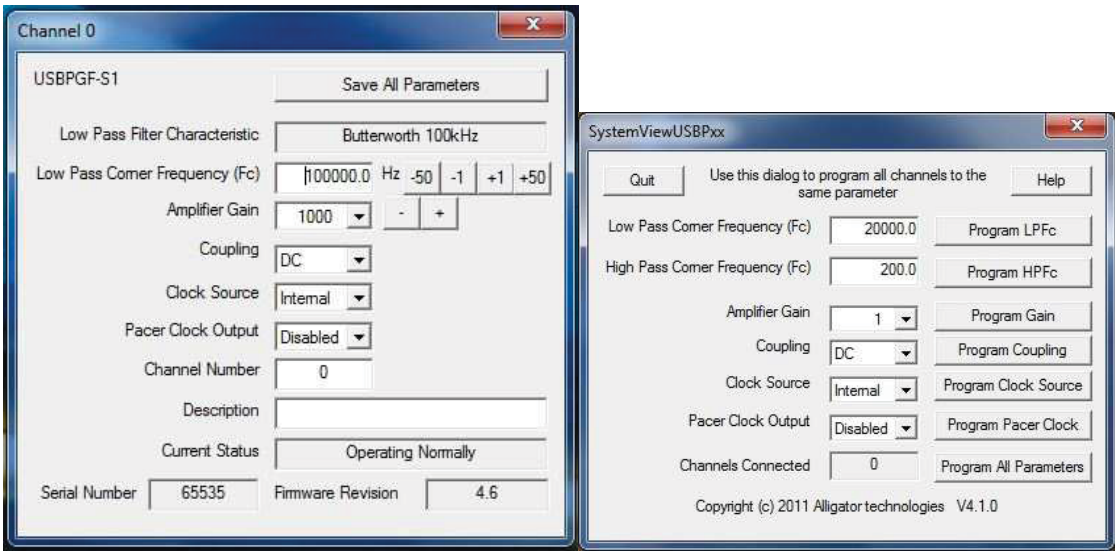


Figure 4-1 Individual device control on the left and global device control on the right

4.2 Operating SystemViewUSBPxx

SystemViewUSBPxx first appears with a dialog centered on the host computers screen. It can be used to control one or more USBPxx-S1 devices. As USBPxx-S1 devices are connected through the USB port of the host computer. The device will be recognized by SystemViewUSBPxx and a single control dialog will be displayed in the upper left corner of the host computers screen. Each subsequent USBPxx-S1 dialog window will be placed in a cascaded fashion relative to the upper left corner. The parameters displayed in the control dialog are a reflection of the current configuration of the USBPxx-S1 device. If a device is disconnected from the host computer, its associated control dialog will disappear from the host computer's screen. Plug it back in and the dialog will reappear.

The Help button will launch Adobe Acrobat Reader with this manual. Adobe Acrobat Reader must be installed for the Help button to operate properly.

The Channels Connected field indicates the number of USBPxx-S1 units connected to the host computer through all of the available USB ports. When a new USBPxx-S1 is connected, this number will

increment and as USBPxx-S1 are disconnected, this number will decrement. If there is a problem registering[1] the USBPxx-S1, then the associated individual control window will not display and the number of USBPxx-S1 modules connected will not show the correct number connected. Check the USB cable and the connection. If using a USBDR-8, make sure that the module is pushed all of the way down into the module connectors. Make sure the connection is snug. Look through the opening in the USBPxx-S1 box at the external clock terminals to see if the red LED is lit. If it is not lit, check the power connection. If power is connected properly and the LED is not lit, then send us an e-mail support@alligatortech.com . If the LED is on and all of the connections seem proper and the USBPxx-S1 still doesn't communicate, then try a different USB port. Try another host computer. Change the USB cable. Exhausted? *Don't* throw the USBPxx-S1 against the wall. Give us a call at (949) 515-1400.

The error code indicates a problem if it is something other than 0. The verbal description of the current status is displayed just below the error code.

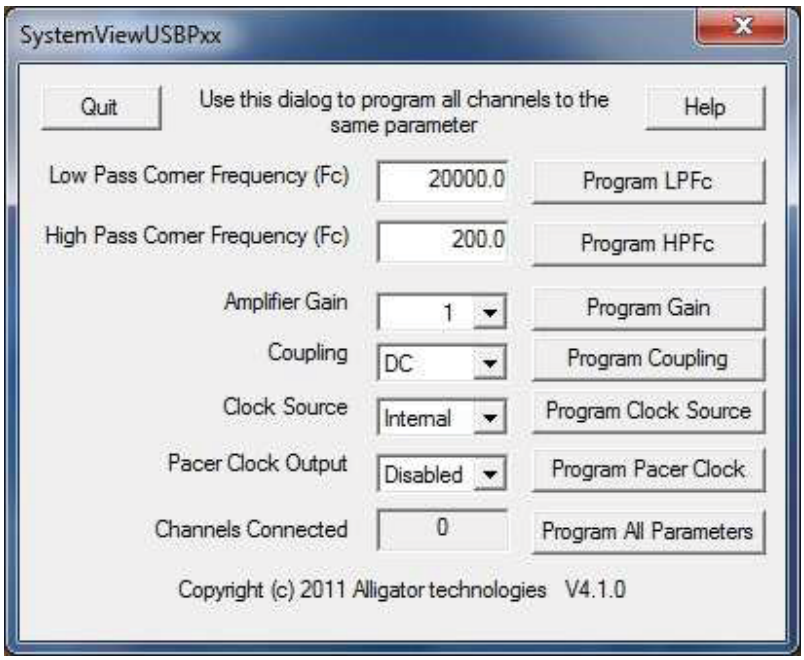
4.2.1 Global Device Controls

There are two ways to globally program all devices simultaneously. Each parameter can be globally updated individually by clicking the control button to the right of the parameter and to program all parameters to all devices, click the **Program All Channels** control button. The individual USBPxx-S1 may not have all of the features present in the global programming dialog, for example the USBPGF-S1 does not have a high pass filter. If a global parameter is modified and then programmed and the individual module does not have the feature, nothing will happen. All simultaneously connected devices that have the feature will update.

[1] The correct USB terminology is to enumerate.

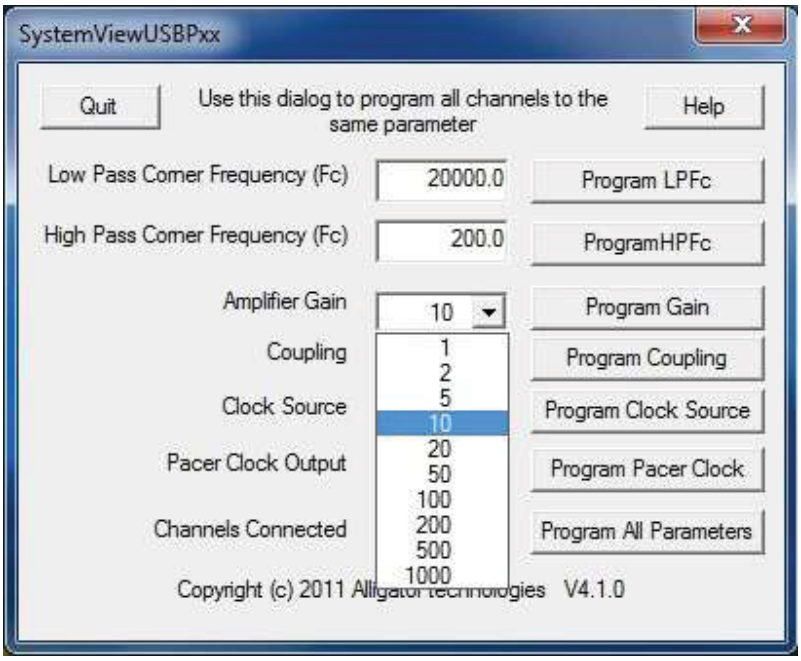
4.2.1.1 Setting a Global Filter Corner Frequency (Fc Hz).

Figure 4-2 Globally Setting of the filter Corner Frequency (Fc)



Update either the low pass or high pass corner frequency and click the respective **Program LPFc** or **Program HPFc** button to the right of the edit box. The allowed range of the low pass filter is from 0.1Hz to the total band width of the installed filter characteristic. The value is in Hz. In other words, a 1kHz Fc must be entered as 1000.0. If a variety of filter characteristics are simultaneously connected and the global low pass frequency exceeds the band width range of the filter type, an error will be displayed in the individual control dialog relative to the channel that has the problem. That unit will not update but all of the other units that are in range will update as expected. The high pass corner frequency range is relative to the high pass filter installed. It operates in the same manner as setting the low pass frequency. If an individual unit is out of range it will display an error.

4.2.1.2 Setting global amplifier gain level

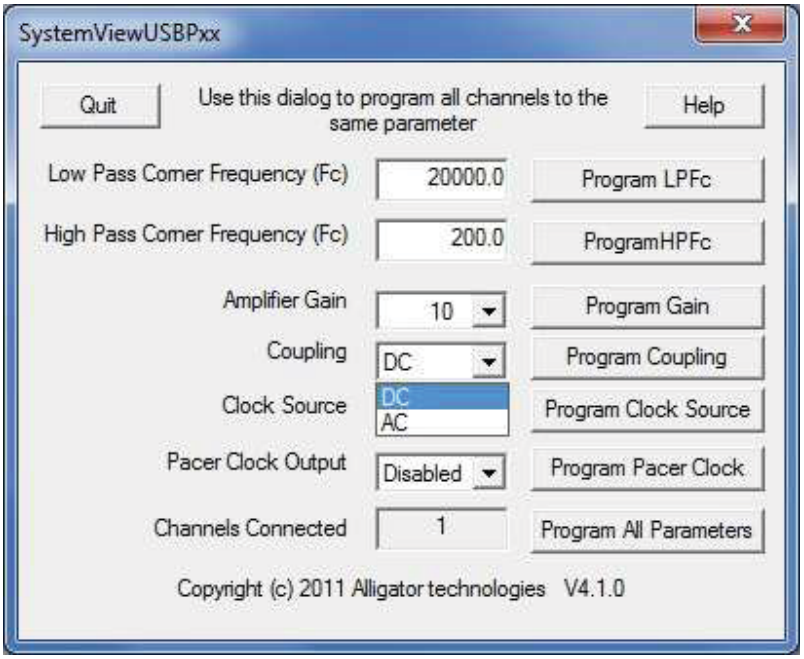


4-3 Globally setting the amplifier gain

Select one of the 10 gain values of the USBPxx-S1 range from 1 to 1,000 from the Amplifier Gain drop down list. Click **Program All Parameters** to write all parameters including gain to all devices or click **Program Gain** to write just the gain selection to all devices. The resulting output signal will have a signal gain of the multiple selected on each channel. In other words, if a gain of 10 is selected and a 0.1Vpp (Volts peak to peak) signal is applied at the input, the output of the pass band frequencies will be 1Vpp. The maximum voltage allowed is 20Vpp centered on 0V. If the amplifier gain is set too high causing the resulting voltage greater than ±10V, the output signal will be clipped and will not extend beyond ±10V.

4.2.1.3 Setting Global AC/DC coupling

4-4 Globally Setting the AC/DC Couple



An AC coupled signal is defined as a signal passed through a series capacitor (very low frequency passive high pass filter) that will remove the DC bias of the input signal. A DC coupled signal is defined as a signal that is not high pass filtered or, allowed to have a DC bias. AC coupling is useful when the input signal is riding on a DC bias large enough to create a situation where the large amplitude frequency components would saturate the USBPxx-S1 and cause the output to be clipped. Applying the AC couple circuit to this signal will center the signal on 0V.

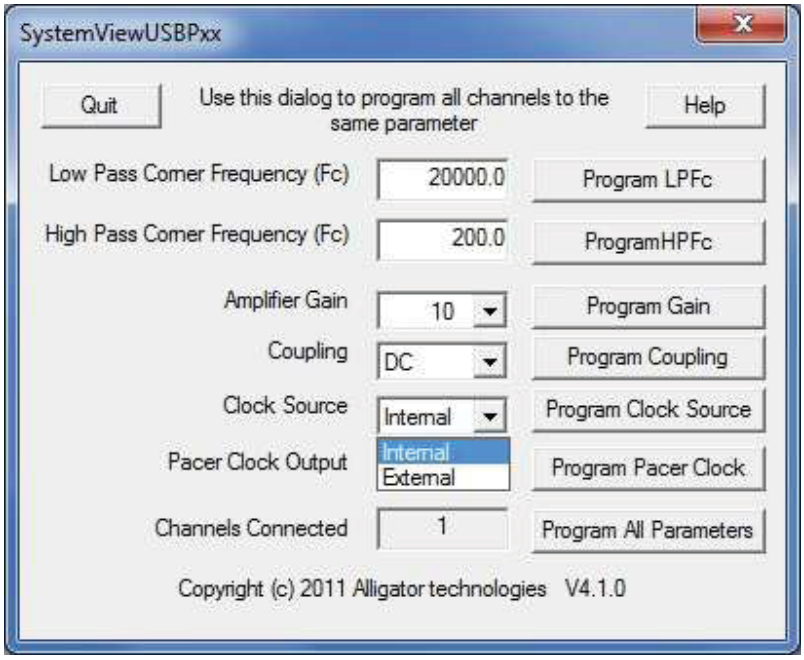
For example let's say we have an input signal of amplitude 2Vpp and it is riding on a +9V DC bias. If this signal was passed through DC coupled, the portion of the 2Vpp signal plus the bias that was in excess of the 10Vmax of the USBPxx-S1 would be clipped. With the AC couple enabled, the signal could then be amplified with a gain of 5 and the output would be an intact 0V centered 10Vpp signal.

To set all channels to be AC coupled, select AC or DC coupling from the drop down list and click **Program All Parameters** or **Program Coupling**.

The AC couple corner frequency is fixed at the factory to be a fraction of a Hz. The factory set corner frequency is desirable in nearly all applications. Please contact the factory for special case modification of the AC couple corner frequency.

Since AC coupling is a passive high pass filter, the USBPBP-S1 and the USBPHP-S1 are equipped with active high pass filters and do not have an AC coupling switch.

4.2.1.4 Setting Global Clock Source



4-5 Globally Setting the Clock Source

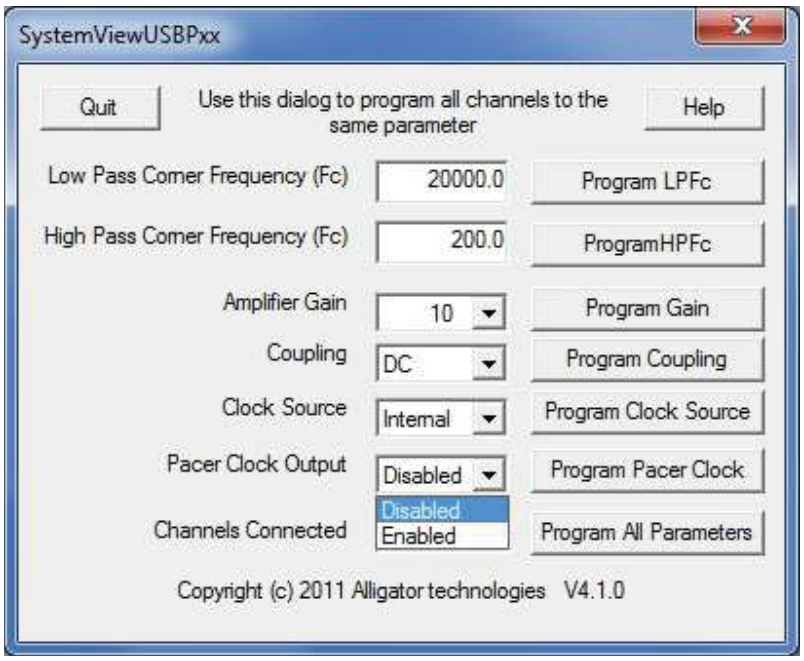
There is an internal clock generator on each USBPGF-S1 and USBPBP-S1 device. The clock frequency (Fclock) controls the filter corner frequency. An alternate control of the Fclock can be selected by connecting an external digital clock source to the clock input of the USBPGF-S1 or USBPBP-S1 and selecting External from the drop down list and then click **Program All Parameters** or **Program Clock Source**.

The external clock should be used in applications where the corner frequency of the filter must be dynamically controlled relative to the input signals frequency components. An example of this would be a rotating shaft. As the shaft rotates slower, the frequency components in the input signal would be lower and the corner frequency of the filter can be lowered. The clock could be generated by a Hall Effect Sensor (HES) mounted on the shaft. The HES will generate a square wave relative to the shaft rate of revolution.

Please refer to Table 3-1 for the relationship of the Fclock to Fc for each filter characteristic.

PLEASE TAKE NOTE: if there is no clock supplied and the external clock input is enabled, the low pass filter in the USBPGF-S1 and USBPBP-S1 will not operate. The output of the filter will drift quickly to the positive or negative power rail. This will saturate the DC offset compensation circuit. When a clock is restored, it will take approximately 90 seconds for the DC offset compensator to recover. We strongly recommend purchasing the USBPGF-S1 or USBPBP-S1 with the DC offset compensation disabled for applications requiring external clock control where the presence of an external clock cannot be guaranteed and the recovery period is not acceptable.

4.2.1.5 Setting Global Pacer Clock Output



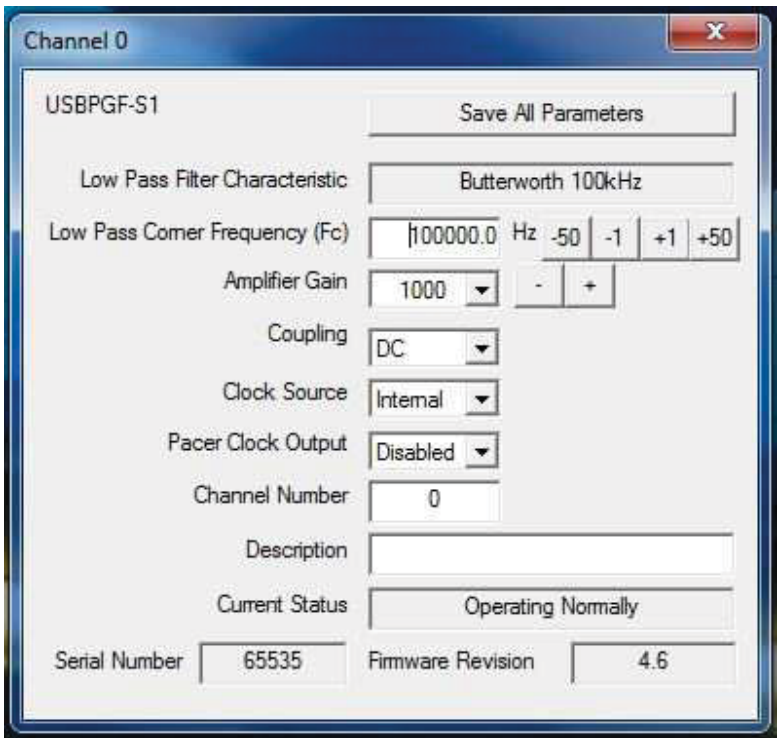
4-6 Globally Setting the Pacer Clock Output

The USBPGF-S1 and USBPBP-S1 have low pass filters that are controlled by an internally generated clock called Fclock. To output the Fclock to the Clk Out pin, select Enable from the drop down list and then click **Program All Parameters** or **Program Pacer Clock**.

The Pacer Clock can be used to synchronize the data collection device with the low pass filter clock. Sampling the output of the low pass filter asynchronously with the filter clock can result but not necessarily produce a small amount of “noise” from sampling error. Synchronizing the A/D with the low pass filter clock will effectively eliminate the sampling error and may increase resolution by as much as 1-bit when using a 16-bit A/D.

4.2.2 Individual Channel Device Controls

Each USBPxx-S1 unit is individually represented by a dialog window cascaded from the upper left corner of the screen in the order that they are attached to the host systems USB ports. When the USBPxx-S1 is attached, it is first quarried for a complete list of stored settings and then the dialog window is displayed with the current configuration of the unit. The drop down lists, edit fields, and check boxes can then be used to change the stored parameters and the **Save All Parameters** button will send the changed values to the specific USBPxx-S1 for permanent storage. Parameters can be changed and the output waveform will simultaneously change as selections are made. The selections are temporary until made permanent with the Save button. Once the parameters are saved, the USBPxx-S1 will operate as expected whether it is connected to the host computer or not. When power is removed and then reattached to the USBPxx-S1 the currently stored configuration is read from non-volatile memory and used as the default configuration.



4-7 The Individual USBPxx-S1 control dialog window

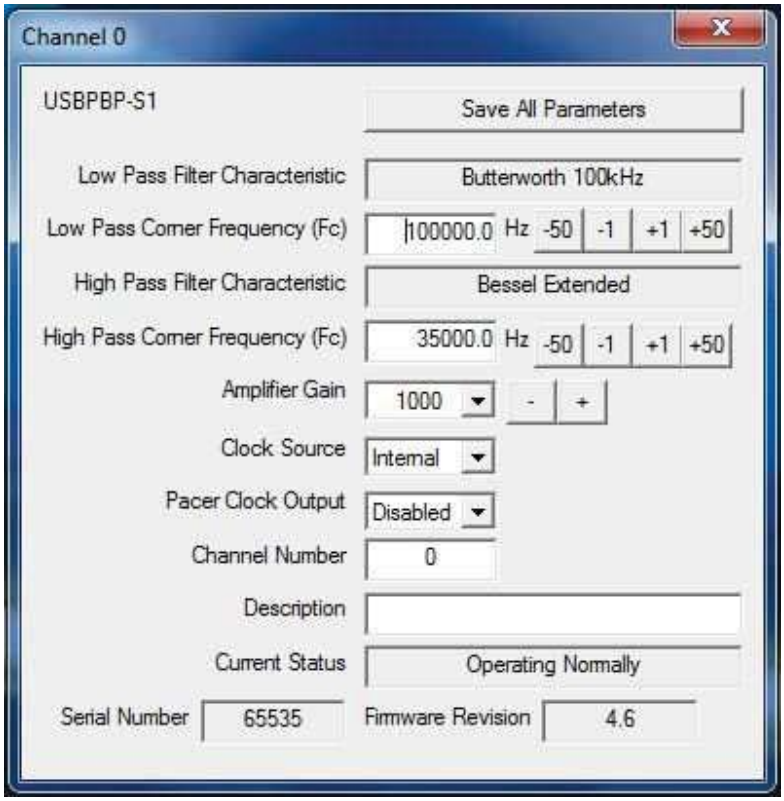
Elliptic bandwidth DC to 50kHz
Elliptic bandwidth DC to 100kHz
Butterworth bandwidth DC to 100kHz
Bessel bandwidth DC to 66kHz
Linear Phase bandwidth DC to 100kHz
Linear Phase bandwidth DC to 200kHz

Table 4-1 The available standard filter characteristics

The Filter characteristic field represents the filter configuration of the USBPGF-S1, USBPBP-S1, or USBPHP-S1 unit. It can only be modified at the factory. Contact us if modification is required. Some of the available filter characteristics can have a modified band width. The standard bandwidths are the widest available for the filter characteristic. There are some advantages to having a narrower bandwidth and particularly the Fclock frequency to Fc ratio is larger by a factor of 2. This can affect tracking filter and clock synchronization applications.

4.2.2.1 Setting an Individual Filter Corner Frequency (Fc Hz).

4-8 Individually Setting of the filter Corner Frequency (Fc)



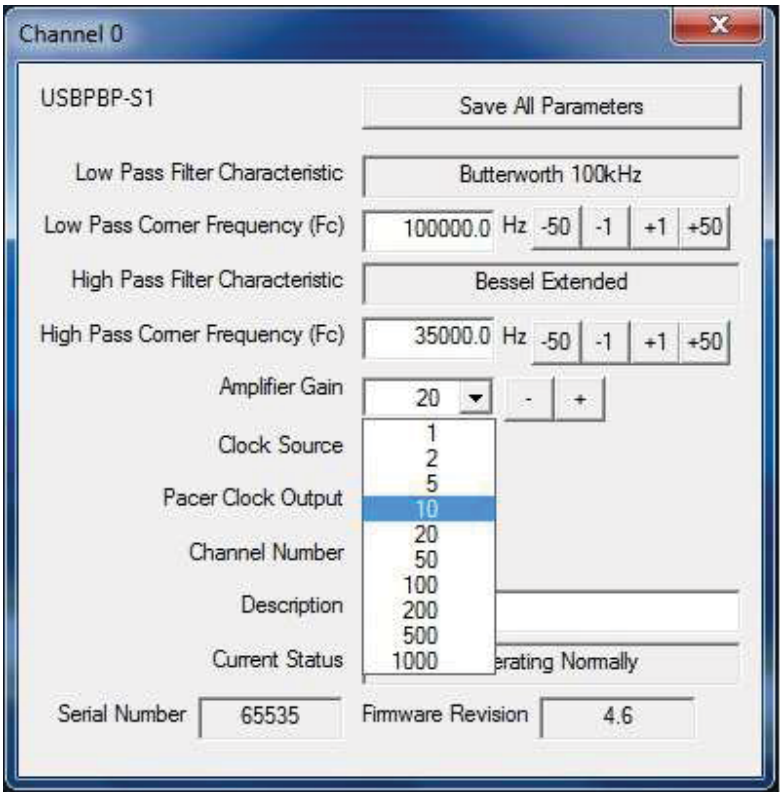
Update the edit box with the corner frequency. The allowed range for the low pass filter is from 0.1Hz to the total band width of the installed filter characteristic. The value is in Hz. In other words, a 1kHz Fc must be entered as 1000.0. The allowed range of the high pass filter is based on the calibration results of the installed filter. If the low pass filter corner frequency is set less than the high pass corner frequency, the output signal may be completely attenuated relative to the overlapping rejection bands.

The increment and decrement buttons to the right of the edit box will add or subtract the button value from the corner frequency in the edit box. The frequency is transmitted to the device on each button click simplifying the fine tuning of the corner frequency.

The edit field represents an approximation of the physical corner frequency. In applications requiring a high degree in accuracy of the physical filter corner frequency, apply a pure tone input signal at the corner frequency desired to the input of the filter, measure the output relative to the input, and adjust the corner frequency up or down using the +1 and -1 buttons until -3dB is measured at the output relative to the input signal. For applications requiring phase accuracy between channels, the corner frequencies of all channels must be matched in this manner. The actual phase between input and output can be used as the calibration criterion. Phase matching of less than 1° between channels can be achieved through calibration utilizing this method.

To permanently save the corner frequency and all other parameters, click **Save All Parameters**.

4.2.2.2 Setting an individual amplifier gain level



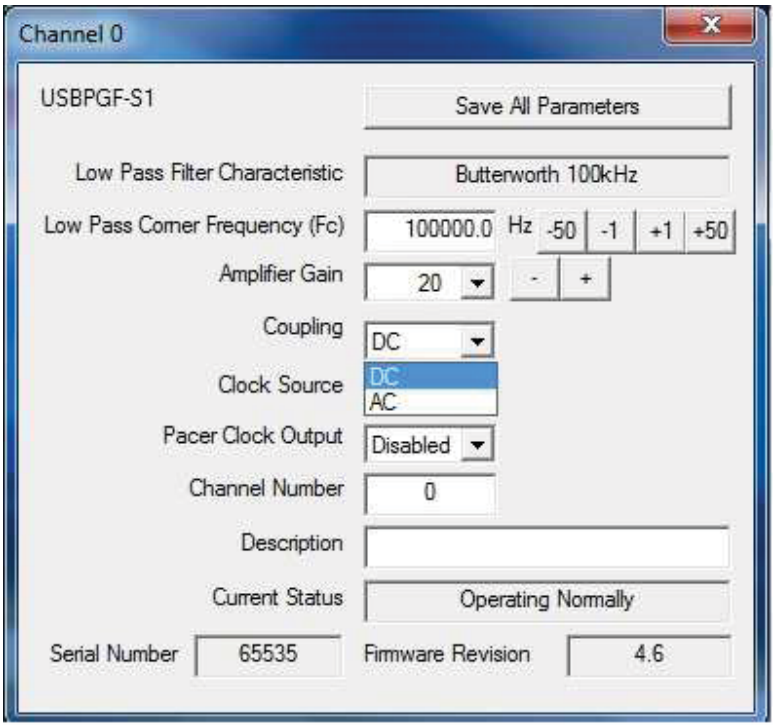
4-9 Individually setting the amplifier gain

Select one of the 10 gain values of the USBPxx-S1 range from 1 to 1,000 from the Amplifier Gain drop down list. The resulting output signal will have a signal gain of the multiple selected on each channel. In other words, if a gain of 10 is selected and a 0.1Vpp (Volts peak to peak) signal is applied at the input, the output of the pass band frequencies will be 1Vpp. The maximum voltage allowed is 20Vpp centered around 0V. If the amplifier gain is set too high causing the resulting voltage greater than ±10V, the output signal will be clipped and will not extend beyond ±10V. The + and – buttons to the right of the drop down list will increment or decrement through the gain list.

To permanently save the gain selection and all of the other parameters, click **Save All Parameters**.

4.2.2.3 Setting an Individual AC/DC coupling

4-10 Individually Setting the AC/DC Couple



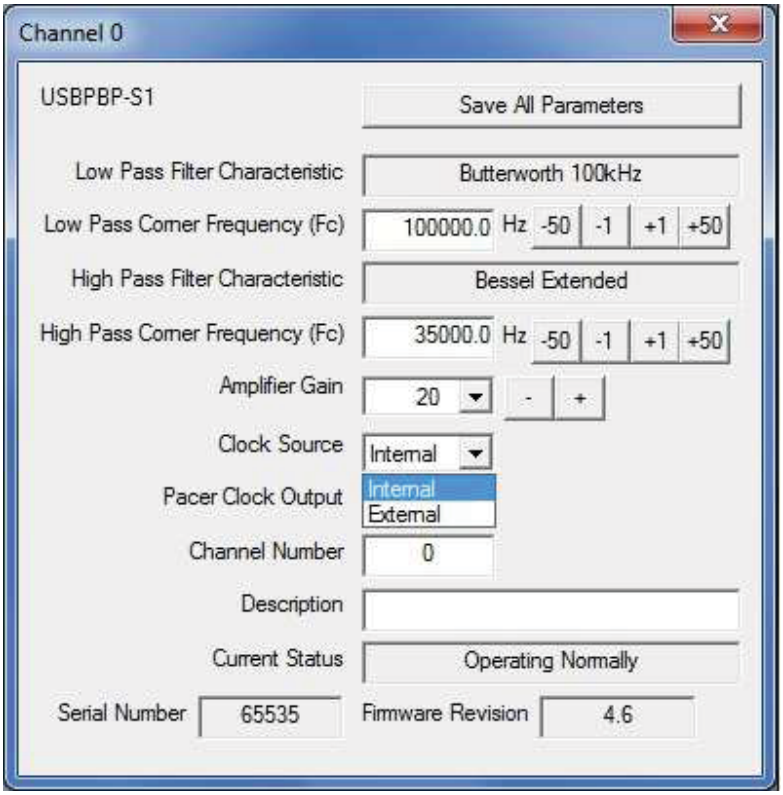
An AC coupled signal is defined as a signal passed through a series capacitor (very low frequency passive high pass filter) that will remove the DC bias of the input signal. A DC coupled signal is defined as a signal that is not high pass filtered or, allowed to have a DC bias. AC coupling is useful when the input signal is riding on a DC bias large enough to create a situation where the large amplitude frequency components would saturate the USBPxx-S1 and cause the output to be clipped. Applying the AC couple circuit to this signal will center the signal on 0V. For example let's say we have an input signal of amplitude 2Vpp and it is riding on a +9V DC bias. If this signal was passed through DC coupled, the portion of the 2Vpp signal plus the bias that was in excess of the 10Vmax of the USBPxx-S1 would be clipped. With the AC couple enabled, the signal could then be amplified with a gain of 5 and the output would be an intact 0V centered 10Vpp signal.

To permanently save the AC coupling selection and all of the other parameters, click **Save All Parameters**.

The AC couple corner frequency is fixed at the factory to be a fraction of a Hz. The factory set corner frequency is desirable in nearly all applications. Please contact the factory for special case modification of the AC couple corner frequency.

4.2.2.4 Setting an Individual Clock Source

4-11 Individually Setting the Clock Source



There is an internal clock generator on each USBPGF-S1 and USBPBP-S1 device. The clock frequency (Fclock) controls the low pass filter corner frequency. An alternate control of the Fclock can be selected by connecting an external digital clock source to the clock input of the USBPGF-S1 or USBPBP-S1 and selecting External from the drop down list.

The external clock should be used in applications where the corner frequency of the filter must be dynamically controlled relative to the input signals frequency components. An example of this would be a rotating shaft. As the shaft rotates slower, the frequency components in the input signal would be lower and the corner frequency of the filter can be lowered. The clock could be generated by a Hall Effect Sensor (HES) mounted on the shaft. The HES will generate a square wave relative to the shaft rate of revolution.

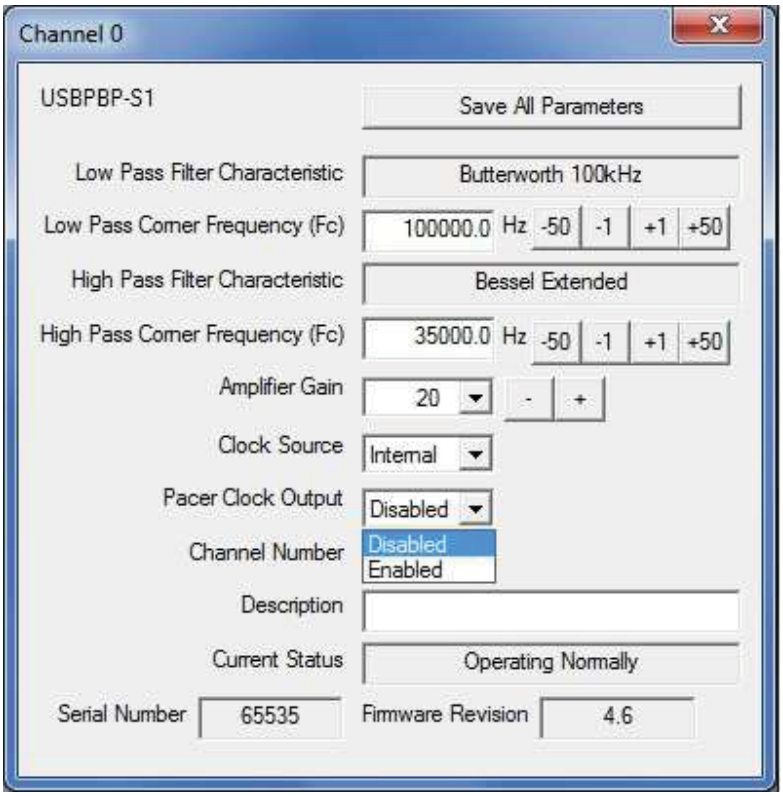
To permanently save the clock source selection and all of the other parameters, click **Save All Parameters**.

Please refer to Table 3-1 for the relationship of the Fclock to Fc for each filter characteristic.

PLEASE TAKE NOTE: if there is no clock supplied and the external clock input is enabled, the low pass filter in the USBPGF-S1 or USBPBP-S1 will not operate. The output of the filter will drift quickly to the positive or negative power rail. This will saturate the DC offset compensation circuit. When a clock is restored, it will take approximately 90 seconds for the DC offset compensator to recover. We strongly recommend purchasing the USBPGF-S1or USBPBP-S1 with the DC offset compensation disabled for applications requiring external clock control where the presence of an external clock cannot be guaranteed and the recovery period is not acceptable.

4.2.2.5 Setting an Individual Pacer Clock Output

4-12 Individually Setting the Pacer Clock Output



The USBPGF-S1 and USBPBP-S1 have low pass filters that are controlled by an internally generated clock called Fclock. To output the Fclock to the Clk Out pin, select Enable from the drop down list.

To permanently save the pacer clock selection and all of the other parameters, click **Save All Parameters**.

The Pacer Clock can be used to synchronize the data collection device with the low pass filter clock. Sampling the output of the low pass filter asynchronously with the filter clock can result but not necessarily produce a small amount of “noise” from sampling error. Synchronizing the A/D with the low pass filter clock will effectively eliminate the sampling error and may increase resolution by as much as 1-bit when using a 16-bit A/D.

4.2.2.6 Channel Number

The channel number can be set to any number and the value is stored in the USBPxx-S1. We suggest using it to indicate which A/D channel is wired to the USBPxx-S1. But, since it is just a descriptive field, feel free to use it for anything. The dialog window title is set to the same number when the USBPxx-S1 is module is Programmed with the **Save All Parameters** button. The USBPxx-S1 will report this number when it is first connected to the host computer and the window will come up with the previously stored value.

4.2.2.7 Channel Description

The channel description is 30 characters long. We suggest using it to describe which sensor is connected to the input of the USBPxx-S1. But, since it is just a descriptive field, feel free to use it for anything. The text will be stored in the USBPxx-S1 when the **Save All Parameters** button is clicked.

5 Achieving Accurate Results Using the USBPGF-S1

5.1 DC Offset

The DC offset introduced by the filter will be ±1.5mV or less. The DC offset compensation circuitry can be disabled (factory implemented option) if the time constant of the circuitry interferes with the dynamics of the input signal.

Whether or not DC offset compensation is disabled the DC offset is calibrated at the factory. The calibrated DC offset can change with age or the nominal operating temperature. If using a DC offset disabled, the DC offset typically can vary from the calibrated and be from ±30 to ±50mV and with some filter types an offset as much as ±175mV may be present. If the principal application is in signal variations such as AC components or if the DC offsets of the system are unimportant, software normalization calibration of DC offset is unnecessary. However, if such software normalization calibration is necessary, this section describes how to do it.

5.1.1 Characterization of the DC Offset

If greater DC offset accuracy is required the adjustment for DC offset must be made through the data acquisition system. To characterize the DC offset, the HI and LO inputs of the channel being tested must be connected together and to analog ground. The channel output voltage is then measured through the A/D board. The simplest procedure is:

- Using the screw terminal connector connect the **In Hi, In Lo,** and **A Gnd** with shunting wires as shown.

5-1 Grounding the input to the USBPxx-S1

- Set the USBPxx-S1 corner frequencies as required and measure the voltages on all channels with the A/D system. If the A/D gains will be used, set them to the same levels as would be used with real input signals.
- Store the resulting voltages on disk. These voltages are the DC offset generated by the USBPxx-S1. Use these values to normalize the actual voltage.

5.1.2 Normalization of the USBPxx-S1 DC Offset

To eliminate the effects of DC offset errors:

- Measure the offset voltage of each channel and save its value as a normalization constant.

- Subtract the normalization constant value from every measurement.

In addition, the DC offset can be reduce by adding adjustment circuits to trim the signal levels, or it can be eliminated entirely by capacitive coupling (a capacitor in series with the signal path) from the USBPxx-S1 to the A/D input. Each solution is explained in more detail in the following sections.

5.1.2.1 Using Adjustment Circuits

If greater DC accuracy and gain accuracy are desired, adjustment circuits may be added for trimming the signal levels.

The best circuit location on an external perf board. The circuit can be made with one operational amplifier per channel. The amplifiers might be connected in a non-inverting circuit with gain and offset trim, as shown in the figure below.

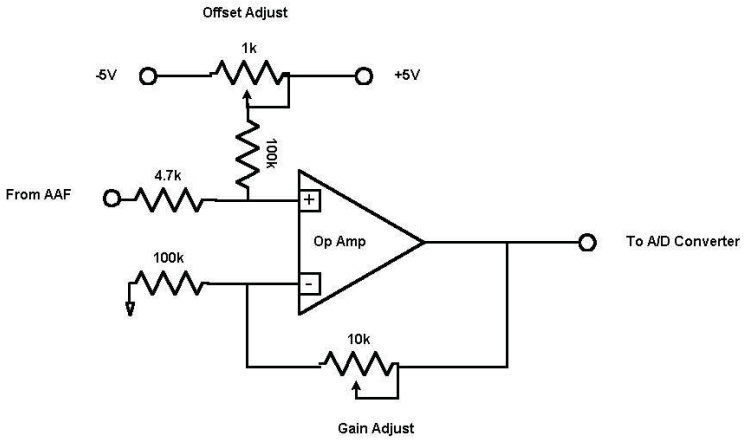


Figure 5-2 Adjustment Circuit for Trimming Signal Levels

The op-amp need not be a high-precision unit. Its offset should be reasonably stable, and its gain-bandwidth product should be 100 or more times the highest filter corner frequency. The power supplies should be well bypassed, capacitively decoupled, close to the op-amp. Typically decoupling capacitors are unpolarized ceramic 0.1μF 5%. Stable resistors, such as 1% metal-film resistors, should be used.

6 Common-Mode Rejection

The common-mode rejection (CMR) is the ratio between the output due to a legitimate differential-mode input and the output due to a common-mode input at the same voltage. The common-mode rejection of the USBPxx-S1 is 75dB minimum, 86dB typical, at low gains, rising to 106dB minimum, 110dB typical at high gains. 75dB is a voltage ratio of 5600 to 1.

In many applications, the extreme CMR available with the USBPxx-S1 is not critical. Some degradation of the CMR would not affect these applications significantly. However, the level of CMR will be critical in other applications.

The usual source of CMR degradation is an impedance imbalance in the signal-source circuit. The USBPxx-S1 input impedance is not infinite. Each input terminal has a 2MΩ resistor to analog ground. This is paralleled by stray and cable capacitance, which can be somewhat unbalanced. The signal source impedance can form a voltage divider with these components. Unless special care is taken, the voltage division ratio will not be the same on both HI nd LO sides, so the CMR may be reduced. Please refer to the figure below.

Since the USBPxx-S1's CMR is so good, even a small amount of conversion to normal-mode

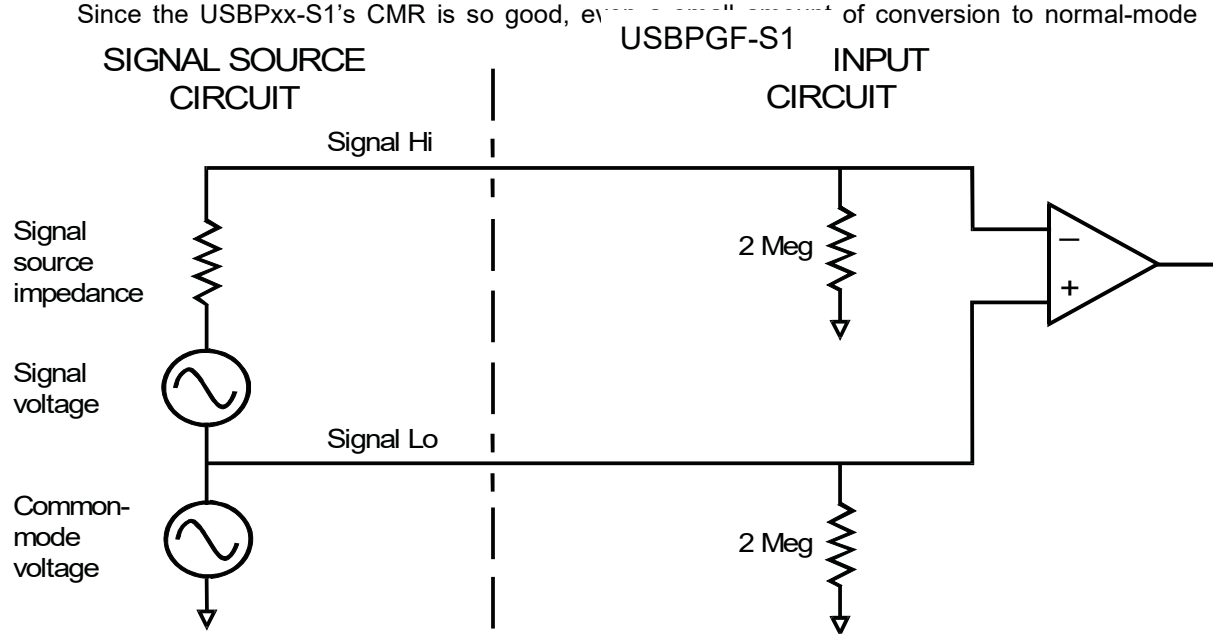


Figure 6-1 Common-Mode Conversion from Non-Zero Source Impedance

voltage by impedance imbalances can be noticeable. The low-frequency CMR of the USBPxx-S1 input circuit is typically better than 90dB or 30,000 to 1 in voltage. Thus, 10 volts of common-mode input should disturb the output by only a fraction of a millivolt. However, as can be seen from the figure above, a 1KΩ source unbalance will convert roughly 1/2000 of the common-mode rejection to 66dB.

Use the figure above to calculate the effect of any source-resistance unbalance. If the common-mode degradation due to source resistance is too great, a trimming resistor may be added to balance it, as shown in the figure below.

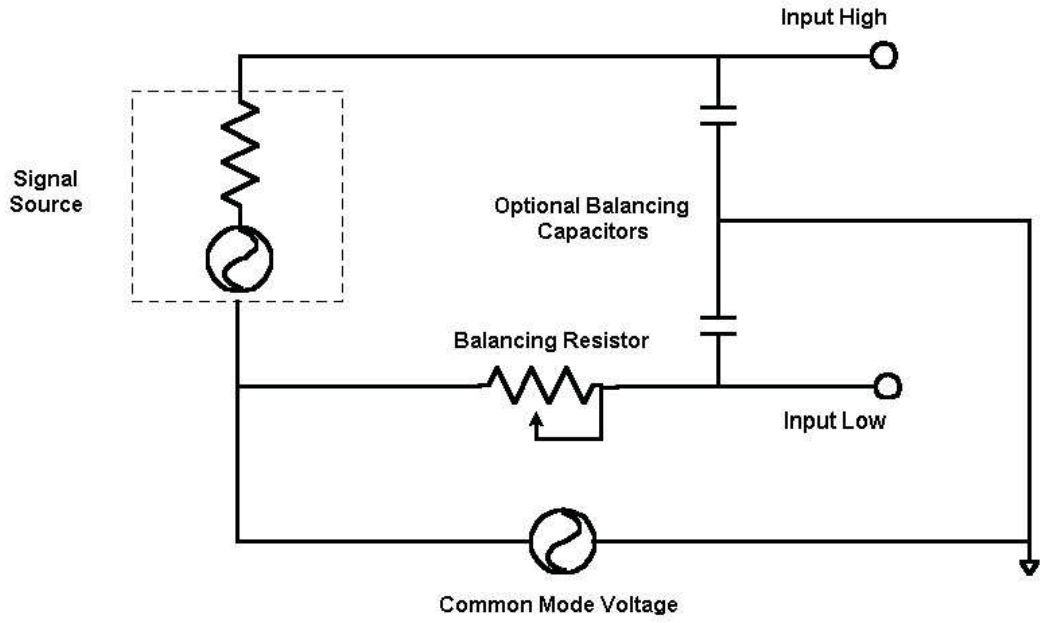


Figure 6-2 Improving Common Mode Performance

If the common-mode voltage is rapidly varying with pulses or high frequencies, the balancing problem may become more difficult. The optional capacitors shown in the above figure may help. The capacitor values should be adjusted to make the signal capacitances to ground equal on both sides. The exact point of introduction of the common-mode voltage may sometimes be obscure, especially if it is coupled by stray capacitances at high frequencies. It may even vary with time, mechanical positioning, etc. In these circumstances, an experimental approach to capacitor and resistor setting may be useful.

In addition to their common-mode effects, non-zero source and trimmer impedances can affect the overall effective gain of the filter. The input signal source is referenced to analog ground through the 2 MΩ input resistors of the USBPxx-S1 channel.

6.1 High-Frequency Clock Aliasing

In the large majority of installations, the USBPGF-S1 filter behaves, as a pure continuous analog device, the inputs and outputs of which are pure analog signals. However, in systems where signals have significant components at typically 100 times the filter corner frequency, the actual nature of the USBPGF-S1 filters should be taken into account.

In place of a traditional active filter, the USBPGF-S1 uses a switched-capacitor filter, which provides for the board's high performance, tunability, and comparatively low cost. A switched-capacitor filter is an analog sampled-data device, in which the signal is quantized in time, but is continuous in amplitude. Its sampling rate is the "filter clock frequency," which is a multiple of the corner frequency.

Significant input signal components between the filter clock frequencies ±1% of the Fc/Fclock ratio can be aliased down into the pass band. Observe the large break in the X-axis values in Figure 7-3. This problem can be eliminated with a "pre-filter."

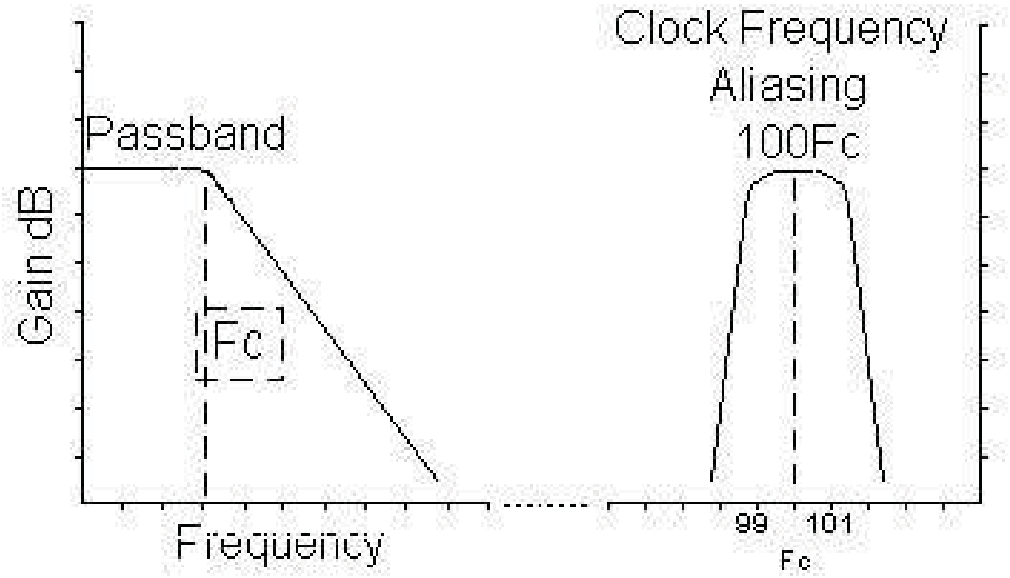


Figure 6-3 The Frequency Response of a Typical Switched-Capacitor Filter

6.1.1 Pre-Filtering

The input of a switched-capacitor filter is, in effect, a sample-and-hold circuit clocked at the filter-clock frequency. Thus, the filter proper sees a sampled analog waveform, not a continuous one. As for any sampled waveform, aliasing can occur if the input signal has high-frequency components. The aliasing occurs around the filter-clock frequency. (Refer to Figure 7-3)

This aliasing is exactly analogous to aliasing of A/D-converter inputs, the prevention of which is the main purpose of the USBPGF-S1.

However, it occurs only for signal components near and above the filter clock frequency. In a majority of systems, the input signals have little or no energy at such high frequencies, so the USBPGF-S1 behaves as if it were a continuous-time filter.

In some systems, the input signal actually does have significant energy at these high frequencies. The high frequency energy could then be aliased back into the filter pass band. In these situations, pre-filtering should be used to eliminate the high frequencies before they reach the main filter.

Note that the "high" frequencies are only those near the filter-clock frequency or its harmonics. For example, if the USBPGF-S1 filter corner is set to 50 Hz using a Cauer elliptic filter type, significant clock-frequency aliasing will be present only for signals between 4950 Hz and 5050 Hz, 9950 and 10050, etc. Other high-frequency components are aliased into the filter stop band, not the pass band, and hence are not visible. Refer to Figure 7-3.

Since the filter-clock frequency is so much higher than the filter's corner frequency, a very simple pre-filter can give good rejection. For example, when needed, a single-pole RC filter with a corner frequency 3 times the USBPGF-S1 corner will attenuate the aliasable energy by a least 30 dB, approximately 33 times in voltage. The factor 3 is chosen to keep the RC pre-filter from causing more than 0.4 dB droop in the USBPGF-S1 pass band. If a 1.5 dB falloff at the high end of the pass band is permissible, the corner frequency could be as low as 1.5 times the USBPGF-S1 corner, giving an additional 6 dB of alias attenuation.

For very severe problems with high-frequency interference, a 2-pole or even 3-pole RC pre-filter, or an active, op-amp, pre-filter could be used.

6.1.2 Application of Pre-Filtering to the USBPGF-S1

Unless a programmable continuous-time filter is used, the pre-filter is optimized for one particular USBPGF-S1 corner frequency. Lowering the USBPGF-S1 corner frequency lowers the clock frequency, which in turn lowers the frequency of aliasable energy. With a fixed pre-filter, this means that the aliasable energy is less well attenuated. Conversely, if the USBPGF-S1 corner frequency is set higher, the fixed pre-filter's response will begin to affect the high end of the USBPGF-S1's pass band although the anti-aliasing effect will actually be enhanced.

If the pre-filter has a relatively sharp corner or if the alias attenuation requirements are not severe, some tuning of the USBPGF-S1 is still feasible. The maximum USBPGF-S1 corner is set by allowable pass band disturbance, e.g. less than 0.4 dB droop at the high end. The minimum USBPGF-S1 corner is set by the desired alias attenuation at the clock frequency.

For example, assume a 2-pole, 12 dB per octave, pre-filter. This gives 36 dB attenuation at 8 times its corner frequency and less than 0.4 dB attenuation at 50% of its corner frequency. If the pre-filter corner were at 10 kHz, the maximum USBPGF-S1 corner frequency with less than 0.4dB high-end droop would be 5 kHz. The minimum USBPGF-S1 corner frequency for at least 36 dB added alias rejection would be 800 Hz.

If full tunability is required, a second USBPGF-S1 channel could be used as a pre-filter. The corner frequency of the second channel would be tuned to, say, 50 times the corner frequency of the final channel. This would make the first clock-frequency-alias point 5000 times the corner frequency of the final channel.

The input buffer amplifier on the USBPGF-S1 board has a single-pole corner at about 400 kHz. This provides minimal automatic anti-alias protection for USBPGF-S1 corners above 10 to 20 kHz.

If required, a pre-filter often can be installed most conveniently with the external signal-conditioning circuits. If this is done, precautions should be taken against pickup noise on the USBPGF-S1 input lines; the pre-filter may increase the input impedance level, making the circuit more susceptible to pickup noise.

If the USBPGF-S1 input is connected single-ended, LO input grounded, one non-critical series resistor in the HI line and one non-critical capacitor to ground will make a single-pole pre-filter. Resistor values less than 10K and preferably less than 1K will reduce the risk of pickup noise or cross talk. Alternatively, a simple op-amp active filter could be used.

If the USBPxx-S1 input is connected in differential mode, care should be taken to avoid degrading the common-mode rejection of the circuit. A differential-mode RC filter requires two equal resistors, one in series with each line, followed by an equal line-to-ground capacitor. Unless they are both less than 100 ohms or so, one of the resistors should be trimmable. The trim resistor should be adjusted for best common-mode rejection. To do this, short the input sides of the resistors together, connect this point to a signal source, and adjust for minimum output from the USBPxx-S1. If op-amp active filtering is used, two identical filters are required, one in each line.

6.2 Post-Filtering

The output of the filter is a high-frequency stair step waveform. It behaves as though a continuous-time filter had been used, followed by a sample-and-hold circuit triggered at the filter-clock frequency.

The stair step waveform is quantized in time, but not in voltage. The duration of each step is one filter-clock cycle. The voltage levels are continuously distributed, not digitized since the filter is an analog sampled-data device.

If the A/D-converter sample frequency is not a synchronous sub-multiple of the filter clock, this quantization will introduce some noise into the A/D-converter readings when the input signal is changing rapidly. The noise is small and can be reduced further by a post-filter, such as a simple RC circuit. The RC corner frequency should be as close to the filter corner as possible, as long as it does not have too much effect within the filter pass band.

If the A/D converter sample frequency is locked to a sub-multiple of the filter clock, the time-quantization noise will not appear, and no post-filter is needed.

The output circuit of the USBPGF-S1 includes a single-pole low-pass RC filter with a corner frequency of about 400 kHz. This is mostly a precaution against high-frequency noise, but it provides automatically some post-filtering for USBPGF-S1 corners above 10 to 20 kHz.

6.3 Input Protection

The input circuit permits normal operation with common-mode voltages up to 40 volts. For normal operation, the differential, normal-mode, input should not exceed the ±5-volt range, or optional 10-volt range. However, transient voltages even high enough to activate the input clipping will cause no damage to the circuit.

The inputs are protected by varistors to analog ground. A varistor is a device that has very high impedance at normal voltages, but low impedance at high voltages. It tends to clip incoming high-voltage transients. In the USBPxx-S1, the varistor clipping level is between 40 to 50 volts. The circuit will withstand transients at this level with no damage.

Applying steady voltages above 40 volts, but below the varistor clipping level, should be avoided. The circuit will withstand such voltages for a few seconds without damage, but reliability of the USBPxx-S1 may be reduced. A long duration of applied high voltage may cause permanent damage. The varistors protect against normal transient pulses such as electrostatic discharge and most switching impulses. However, there is a limit to their energy absorbing capacity. This must be considered if the high-voltage transients come from a low-impedance source. The circuit may be damaged if one transient deposits more than 2 joules or if repeated transients result in a steady-state dissipation of more than 0.1 watt. For example, the circuit would not be protected against a short circuit to a 110 VAC power line. This is because a power line is a very low-impedance source and can deliver large amounts of energy.

All protection is referred to analog ground. As one aspect of normal safety precautions, analog ground should be connected to a good earth ground. Usually, this is done with a single point connection to digital or power ground, which in turn is connected to earth ground. Most A/D converter devices already contain such a connection. See 0 for more information.

If the USBPxx-S1 is disconnected from the A/D board, the earth ground connection is broken. Therefore, as another aspect of normal safety precautions, disconnect the signal source connector before disconnecting the cable at either the USBPxx-S1 or the A/D board.

6.4 Cross talk

Cross talk is a disturbing signal picked up by one channel due to an AC voltage on another channel.

For the USBPxx-S1, the coupling path is normally stray capacitance in circuits or wiring. The coupling capacitance and the receiving circuit impedance form a voltage divider for the disturbing AC signal. High-frequency signal sources always involve a danger of cross talk to other channels whose source impedance is high. This is true regardless of whether an USBPxx-S1 is in the circuit.

The outputs of the USBPxx-S1 filters have a low source impedance of less than 50 ohms. Therefore, with reasonable precautions against radio-frequency noise, megahertz and above, the output of any USBPxx-S1 filter channel should receive negligible cross talk. Cross talk susceptibility on USBPxx-S1 filter inputs and on A/D channels that are in the cable but not filtered depends on their source impedances. Unfiltered channels do not use the USBPGF-S1 at all. The actual amount of cross talk will depend on the frequency and amplitude of the disturbing signal, and on the distributed capacitance of the signal and connection cables.

Keeping signal source impedances reasonably low can essentially eliminate capacitive cross talk. In severe cases, it can also be helpful to use shielded cable. Unshielded cable may have a distributed cross talk capacitance of tens of Pico farads per foot. The USBPxx-S1 may add a few Pico farads to as much as 20 Pico farads, depending on channel proximity to the total capacitance.

Unused unconnected input channels may show what appears to be extreme cross talk. This is

because an unused input has practically infinite source impedance. It has no effect on normal operation.

6.5 Physical Environment

The USBPxx-S1 is specified to operate properly over a temperature range of 0°C to 70°C. It can be expected to operate wherever typical PC-compatible computer equipment operates.

As with any electronic equipment not designed for extreme environments, the USBPxx-S1 reliability and operability may be affected by exposure to moisture or airborne chemicals, excessive dirt, fungus growth, severe shock or vibration, or extremely high humidity, close to 100%. Operation at temperatures well below the maximum will improve reliability.

6.6 Electrical Environment

The USBPxx-S1 will operate correctly at relatively high common-mode voltages and will withstand even higher voltages without damage. Every USBPxx-S1 is tested at the factory for proper input impedance at 40 volts input. It is also tested with an 80 volt peak input through 100k Ohms to verify transient clipping levels and assure no breakdown below the clipping level.

The USBPxx-S1 is not designed to Underwriters' Laboratories (UL) physical requirements for high-voltage circuits. The UL requirements are suitable for situations where high-power sources, dirt, extreme humidity, and user abuse may be present. Therefore, the UL specifies large physical space between components. These UL spacing requirements are impossible to incorporate on a board with the size and functionality of the USBPxx-S1.

7 Filter Characteristic Overview

The USBPxx-S1 utilize high performance low pass filters that are optimized for 16-bit applications.

7.1 Features

7.1.1 Sixteen (16) Bit Performance

Circuit DC offset, offset drift, and offset changes are adjusted, and controlled to provide 16-bit performance over the entire operational range of corner frequency and temperature.

7.1.1.1 Automatic DC Offset

The USBPGF-S1 includes an active compensation circuit that automatically compensates for all DC offset changes of the Filter (see the Block Diagram). This circuit eliminates DC offset changes due to time, and temperature. The automatic DC Offset compensation circuit may be disabled with a factory modification.

7.1.1.2 Factory Calibration

To provide optimum performance, factory calibration of both gain and DC offset are provided.

Gain: Gain is adjusted to 0.001dB at a test frequency of 1 kHz, 2.5Vpp and a gain of 1.

DC Offset: Although the Automatic DC offset correction circuit provides compensation for offsets in the Filter Block, it does not provide correction for the offsets associated with the input amplifier. The USBPGF-S1 is factory calibrated for a total DC offset of 0.1mV @ 25°C.

7.1.1.3 Lower Noise

The filters IC used for the USBPGF-S1 are switch capacitor type. These filters sample the input signal, process the signal, and then reconstruct the signal using zero order hold. This process introduces possible aliasing errors and clock feed-through errors.

The USBPGF-S1 includes both pre and post filters that reduce the effects of input aliasing and clock feed-through.

7.1.1.4 Lower Output Impedance

The lower the output impedance, the less influence external signals will have on the output signal of the filter.

The USBPxx-S1 features output impedance of less than 0.001 ohms.

7.2 Block Diagram

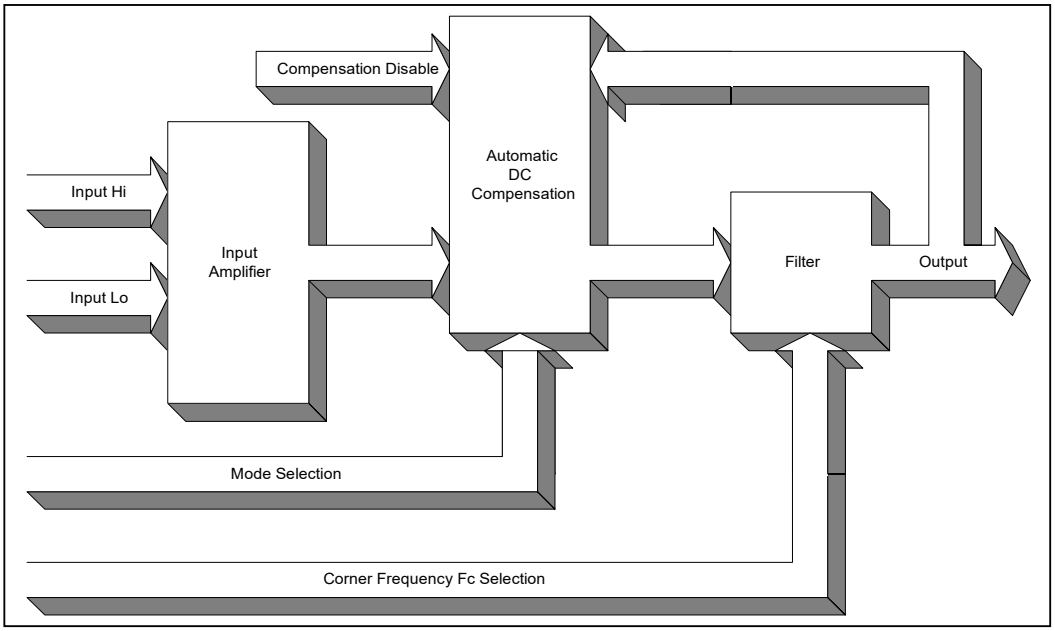


Figure 7-1 USBPGF-S1 Block Diagram

8 USBPGF-S1 General Operation

The block diagram shown above is used for all USBPGF-S1 filter types. The filter may be operated with the automatic DC compensation enabled, or disabled.

8.1 Compensation Enabled

When enabled, an active feed back circuit maintains the filter DC offset. This circuit corrects for DC offset drift due to changes in the operation of the filter circuit. Automatic DC offset circuit causes the Filter to have a gain increase at corner frequencies between 1Hz < F_c 10Hz. The Automatic DC offset also has a time constant of approximately 10 seconds. If for some reason, the input amplifier was to saturate for a long period of time, then the signal reapplied, the time constant would manifest itself by slowly settling the DC level of the output signal to zero. This settling time is in the order of 100 or more seconds, depending upon the desired resolution.

8.2 Compensation Disabled

When disabled, the filter will operate at F_c down to 0.1Hz, although it will have considerable DC offset that will vary with filter corner frequency, and temperature. No time constants are involved with compensation disabled. See **Error! Reference source not found.**, for installation of the jumpers.

8.3 Settling Time

The USBPGF-S1 Automatic DC Compensation circuit requires a significant time to recover from an overload condition. The circuit is governed by the equation:

$V_f = V_i\ (e^{(t/T)})$

Where:
V_f is the final value of the DC offset
V_I is the initial overload voltage
T is the circuit time constant (10 seconds)

Assume the circuit is overloaded, or the inputs are driven to cause input amplifier overload. The input amplifier can drive to the power supply rails, which is 12 volts. Once the system resolution is chosen (bits) the equation is solved for the time required to settle to one LSB of the system resolution.

Initial Overload	12	12	12	12	12
Number of bits	12	13	14	15	16
Voltage Peak	5	5	5	5	5
Volts/Bit	0.002441	0.001221	0.00061	0.000305	0.000153
Settling time (seconds)	85	91	98	105	112

8.4 Corner Frequency F_c Selection

The corner frequency of the filter is selected by applying a square wave clock to the filter module. The filters require a clock that is 25 to 150 times the corner frequency. Clock waveform shape, symmetry, and rise time are all critical to meeting the filter performance specifications.

9 Filter Types

The USBPGF-S1 is available with several different filter types as factory installed options. Each response type has specific characteristics, which must be carefully considered for the application.

9.1.1 Elliptic (Cauer)

The Elliptic filter has ripple in both the pass band and stop band, but provides the fastest transition of any filter type. It has the largest phase nonlinearity, especially near corner. The step response has the largest overshoot and ringing. This filter is offered with 50kHz maximum bandwidth (narrowband software setting).

9.1.2 Butterworth

The Butterworth filter has a maximally flat frequency response. The transition is 160dB/decade, which is second only to the Elliptic filters. The step response has approximately 15% overshoot, and ringing that lasts for a considerable time. The phase response is non-linear, and has the greatest changes from 0.8 F_c to 2 F_c. This filter is offered with 50kHz or 100kHz maximum bandwidth (narrowband or wideband software setting).

9.1.3 Bessel

The Bessel filter is the time domain equivalent of the Butterworth filter. The Bessel filter exhibits droop in frequency domain. The droop is predictable and can be compensated in software by adding appropriate gains verses frequency. The Bessel filter has the slowest transition band of any of the filters at 110dB/ Decade The Bessel filter is maximally flat in the time domain, and exhibits less than 1% overshoot. The Bessel filter exhibits linear phase, with constant group delay to about 1.8 F_c. This filter is offered with 50kHz or 100kHz maximum bandwidth (narrowband or wideband software setting).

9.1.4 High-Speed Elliptic (Cauer)

This filter is similar to the Elliptic (Cauer) filter but is optimized for operation up to 100kHz. In addition, the filter may be operated as either an Elliptic, or as a transitional Butterworth/Elliptic.

When operated in wideband mode, the filter exhibits Elliptic characteristics and has ripple in both the pass band and stop band, but provides the fastest transition of any filter type. The corner frequency goes to 100kHz. It has the largest phase nonlinearity, especially near corner. The step response has the largest overshoot and ringing.

When operated in narrow band mode, the filter exhibits a Butterworth/Elliptic characteristic. The maximum corner frequency is 50kHz. The filter exhibits lower noise and lower delay nonlinearity than the wideband response.

9.1.5 Linear Phase

The Linear Phase filter approximates a maximally flat frequency response. The Linear Phase filter's transition band is faster that the Bessel. At 2 F_c the Bessel filter has 12dB of attenuation, while the Linear Phase has 34dB, and at 3 F_c, the Bessel has 30dB, and the Linear Phase 68dB. The Linear Phase filter is optimized for constant group delay out to about 2 F_c. The time domain response has approximately 5% overshoot with no ringing. The Linear Phase filter is a good choice for a compromise filter that works well in both the time domain and frequency domain. One drawback to the Linear Phase filter is at higher corner frequencies the filter amplitude response has up to 1dB of gain. To maintain a given distortion level, the input signal level must be reduced at high corner frequencies. This filter is offered with 50kHz or 100kHz maximum bandwidth (narrowband or wideband software setting).

9.1.6 Hi-Speed Linear Phase

This filter is similar to the Linear Phase filter, but is optimized for speed. The frequency response is maximally flat. The transition band is not as fast as the Linear Phase, but is still better than the Bessel. The step response has approximately 5% overshoot, and no ringing. The phase response is not as

accurate as the Linear Phase, and shows some deviation, less than 1% from linear over the band to 2 F_c. This filter exhibits significant gain peaking at higher corners. This gain peaking can be as much as 1dB depending upon temperature, with the greater peaking happening at higher temperatures. This filter is offered with 100kHz or 200kHz maximum bandwidth (narrowband or wideband software setting).

10 Specifications

10.1 Power Requirements

10.1.1 USBPxx-S1

+9 to 12V@ 500 mA Maximum

10.2 Input Amplifier

Description	Specification
Voltage range	±10V
Protection	±40V
Common mode rejection	80dB min, 86dB typ
Common mode Voltage	±10V
Noise (RTI)	10ηV per √Hz
DC offset, Factory Adjusted	<±. 0.01mV
DC offset vs temperature	<±20 µV/°C
DC offset, long term drift	<±5µV/Month
Input Impedance	10MΩ/20pF
Input bias current	±2 ηA type, ±5 ηA max
Input offset current	±1 ηA type, ±5 ηA max
Amplifier slew rate	4.0 V/µsec typ, V_o=±5 V
Amplifier bandwidth	1.3 MHz typ

10.3 USBPGF-S1-CE, Elliptic (Cauer)

Filter Characteristics			
Type		Elliptic (Cauer)	
Filter Order		8	
Clock Ratio		100:1	
Chip type		LTC1064-3	
Corner Frequency	Passband Performance	Transition Band, Typ	Stopband Rejection
10Hz to 50kHz	+0.35dB, -0.25dB max -1.25dB, 0.85dB @ F_c	@1.5 F_c = -72dB	-72dB Typ
Wideband Noise		165µV RMS Typ	
Gain			
Accuracy @ 1kHz		0.001%	
THD @input = 3Vrms @ 1kHz		.03%	
Output			
Impedance		.001Ω	
Voltage range		±5V Typical,	
Power Requirement (±12V)			
Typical		32 mA	
Maximum		56 mA	

10.4 USBPGF-S1-B, Butterworth

Filter Characteristics			
Type		Butterworth	
Filter Order		8	
Clock Ratio Narrowband		100:1	
Clock Ratio Wideband		50:1	
Chip type		LTC1064-2	
Corner Frequency	Passband Performance	Transition Band, Typ	Stopband Rejection
10Hz to 50kHz Narrowband 10Hz to 100kHz Wideband	+.15dB, -.5dB max -3.8dB, -2.75dB @ F_c	-48dB Octave	-80dB Typ
Wideband Noise		80µV RMS Typ	
Phase Match		±1.4%° Unit to Unit over @ 20kHz F_c	
Gain			
Accuracy @ 1kHz		0.001%	
THD @input = 3Vrms @ 1kHz		.03%	
Output			
Impedance		.001Ω	
Voltage range		±5V Typical,	
Power Requirement (±12V)			
Typical		34 mA	
Maximum		60 mA	

10.5 USBPGF-S1-L, Bessel

Filter Characteristics			
Type		Bessel	
Filter Order		8	
Clock Ratio Narrowband		150:1	
Clock Ratio Wideband		75:1	
Chip type		LTC1064-3	
Corner Frequency	Passband Performance	Transition Band, Typ	Stopband Rejection
10Hz to 33kHz Narrowband 10Hz to 66.7kHz Wideband	+.15dB, -.5dB max -3.8dB, -2.75dB @ F_c	@3 F_c = -29dB @5 F_c = -60dB	-84dB Typ
Wideband Noise		60µV RMS Typ	
Phase Match		±1.3%° Unit to Unit over full bandwidth	
Gain			
Accuracy @ 1kHz		0.001%	
THD @input = 3Vrms @ 1kHz		.03%	
Output			
Impedance		.001Ω	
Voltage range		±5V Typical,	
Power Requirement (±12V)			
Typical		28 mA	
Maximum		60 mA	

10.6 USBPGF-S1-HC, High-Speed Elliptic (Cauer)

Filter Characteristics			
Type	Hi-Speed Elliptic (Cauer)		
Filter Order	8		
Clock Ratio Narrowband	100:1		
Clock Ratio Wideband	50:1		
Chip type	LTC1064-4		
Corner Frequency	Passband Performance	Transition Band	Stopband Rejection
10Hz to 50kHz Narrowband 10Hz to 100kHz Wideband	+.1dB, -.5dB max -5.75dB, -3.75dB @ F_c Narrowband -4.5dB, -2.5dB @ F_c Wideband	@1.7 F_c = 60dB @2 F_c = 80dB @2.5 F_c = 92dB	90dB Typ
Wideband Noise	135µV RMS Typ		
Phase Nonlinearity	±2° over full operating temperature		
Phase Match	±3%° Unit to Unit over full bandwidth		
Gain			
Accuracy @ 1kHz	0.001%		
THD @input = 3Vrms @ 1kHz	.03%		
Output			
Impedance	.001Ω		
Voltage range	±5V Typical,		
Power Requirement (±12V)			
Typical	28 mA		
Maximum	60 mA		

10.7 USBPGF-S1-LP, Linear Phase

Filter Characteristics			
Type		Linear Phase	
Filter Order		8	
Clock Ratio Narrowband		100:1	
Clock Ratio Wideband		50:1	
Chip type		LTC1064-7	
Corner Frequency	Passband Performance	Transition Band	Stopband Rejection
10Hz to 50 kHz Narrowband 10Hz to 100 kHz Wideband	+.65dB, -.6dB max -2dB, -.35dB at .75 corner -5.75dB, -3.75dB @ F_c Narrowband -4.5dB, -2.5dB @ F_c Wideband	@2 F_c = 34dB @3 F_c = 68dB	90dB Typ
Wideband Noise		115µV RMS Typ	
Phase Nonlinearity		±2° over full operating temperature	
Phase Match		±3%° Unit to Unit over full bandwidth	
Gain			
Accuracy @ 1kHz		0.001%	
THD + Noise		72dB over 50kHz passband	
Output			
Impedance		.001Ω	
Voltage range		±5V Typical,	
Power Requirement (±12V)			
Typical		28 mA	
Maximum		60 mA	

10.8 USBPGF-S1-HLP, Hi-Speed Linear Phase

Filter Characteristics			
Type	Hi-Speed Linear Phase		
Filter Order	8		
Clock Ratio Narrowband	50:1		
Clock Ratio Wideband	25:1		
Chip type	LTC1264-7		
Corner Frequency	Passband Performance	Transition Band	Stopband Rejection
10Hz to 100kHz Narrowband 10Hz to 200kHz Wideband	+.4dB, -.2dB max .85dB at corner	@2 F_c = 28dB @3 F_c = 55dB	90dB Typ
Wideband Noise	175µV RMS Typ		
Phase Match	±1° Filter to Filter		
Gain			
Accuracy @ 1kHz	0.001%		
THD	65dB over 100kHz passband		
Output			
Impedance	.001Ω		
Voltage range	±5V		
Power Requirement (±12V)			
Typical	28 mA		
Maximum	60 mA		

11 Selecting The Right Filter

To select the correct filter for the application it must be decided whether the data is to be analyzed in the time domain or in the frequency domain.

11.1 Time Domain

When analysis is accomplished in the time domain, the filter characteristics that are of utmost importance is the step response. Usually, when analysis is accomplished in the time domain, the most desirable step response is one that follows the input signal as closely as possible with little or no overshoot, and a fast settling time.

The class of filters that meets this requirement has maximally flat time domain response. The Bessel filter was derived to meet this requirement. Unfortunately, the Bessel filter has absolutely the slowest transition response in the frequency domain. The Bessel filter has very poor selectivity in the frequency domain, because it has such a slow roll off.

A second filter type is an optimized type, which does not have a classical transfer function. This filter is called Linear Phase. The Linear Phase filter is optimized for linear phase, but allows some overshoot in the time domain. The frequency response is much better than a Bessel filter. The linear phase filter is a very good compromise between time domain response and frequency response.

11.2 Time Domain Response

11.2.1 Step Response, Elliptic (Cauer)

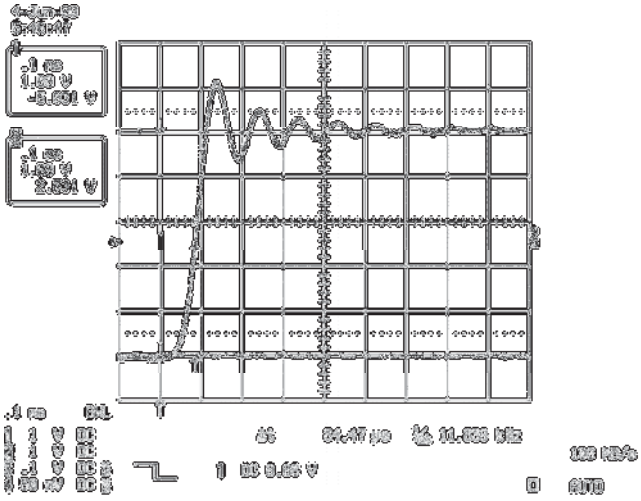


Figure 11-1: Elliptic (Cauer), 10kHz Corner

The Elliptic filter has the largest overshoot and the longest settling time of all the classical filters. Filter delay is nonlinear especially near the corner frequency.

11.2.2 Step Response, Butterworth

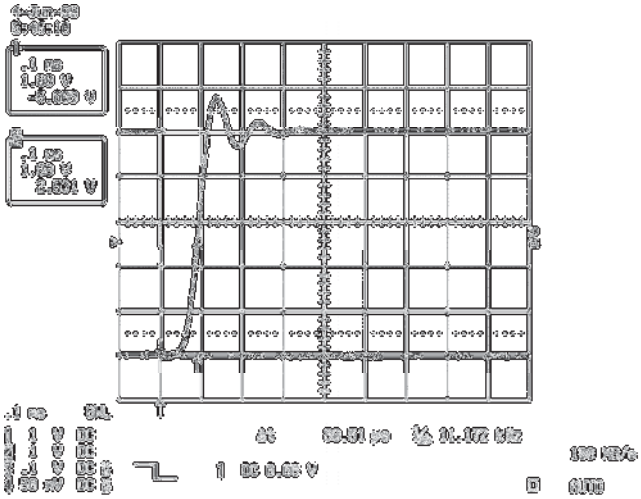


Figure 11-2: Butterworth, 10 kHz Corner, Narrowband

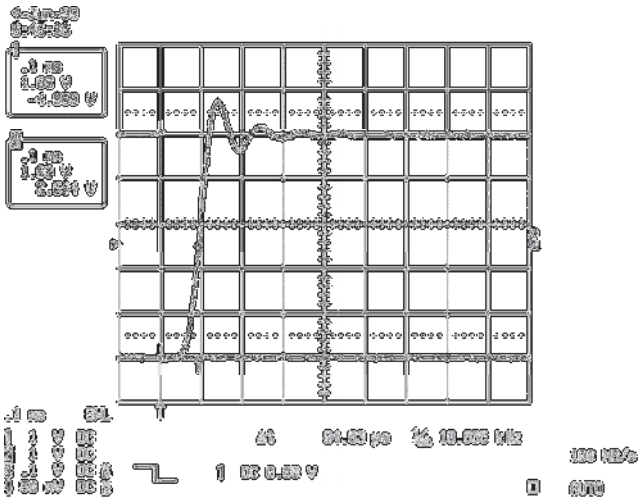


Figure 11-3: Butterworth, 10 kHz Corner, Wideband

The Butterworth filter is second only to the Elliptic filter, and for our 8th order filter, has approximately 15% overshoot. Settling time is on the same order as the Elliptic filter.

The Butterworth filter exhibits the same step response characteristics in both Narrowband and Wideband modes.

11.2.3 Step Response, Bessel

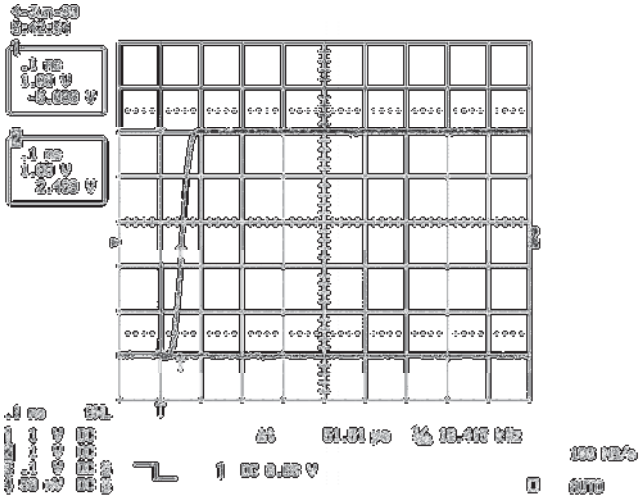


Figure 11-4: Bessel, 10 kHz Corner, Narrowband

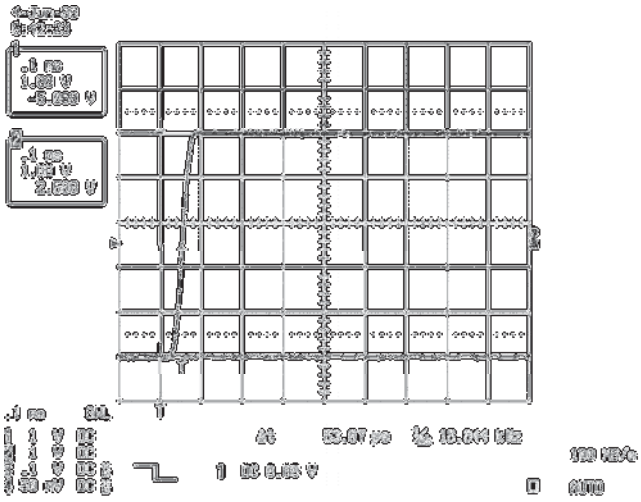


Figure 11-5: Bessel, 10 kHz Corner, Wideband

The Bessel filter has almost no overshoot and minimal settling time of all the classical filters.

11.2.4 Step Response, Hi-Speed, Elliptic (Cauer)

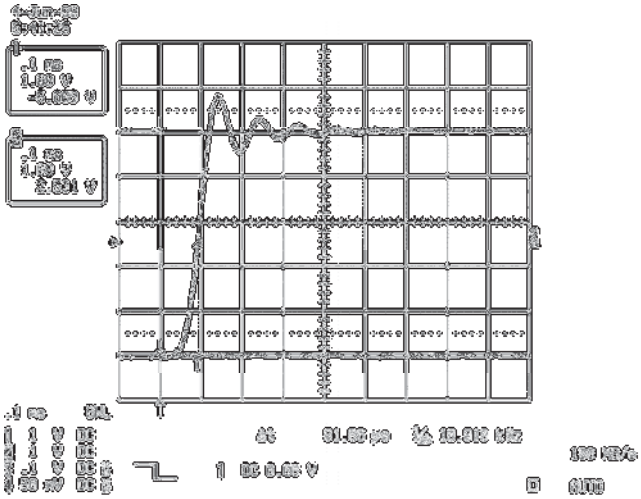


Figure 11-6: Hi-Speed, Elliptic (Cauer), 10 kHz Corner, Narrowband

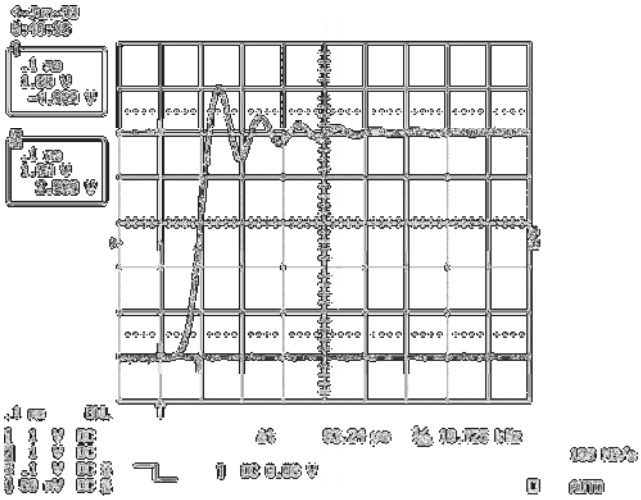


Figure 11-7: Hi-Speed, Elliptic (Cauer), 10 kHz Corner, Wideband

The Hi-Speed Elliptic filter has a response very similar to the Elliptic filter.

11.2.5 Step Response, Linear Phase

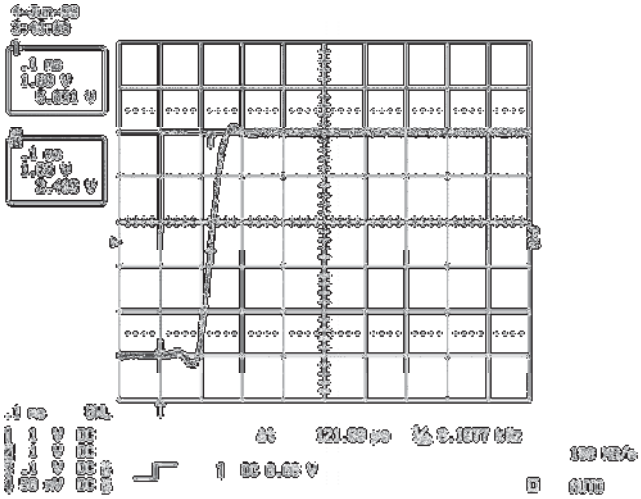


Figure 11-8: Linear Phase, 10 kHz Corner, Narrowband

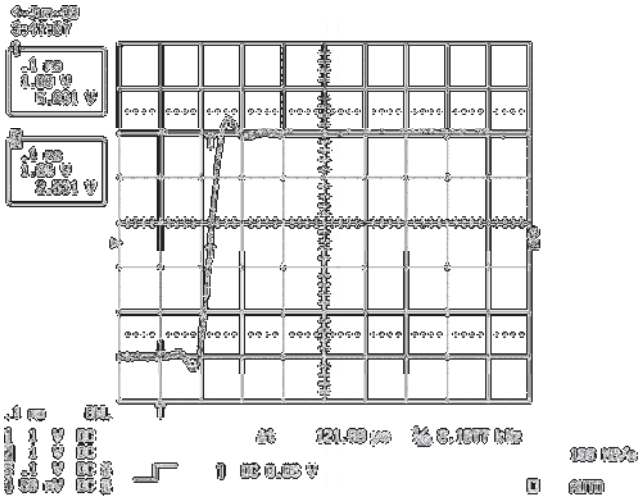


Figure 11-9: Linear Phase, 10 kHz Corner, Wideband

The Linear Phase filter is a compromise filter that has approximately 5% overshoot in the step response. Notice that in the wideband mode the step response overshoots a bit more that in the narrowband mode.

11.2.6 Step Response, Hi-Speed Linear Phase

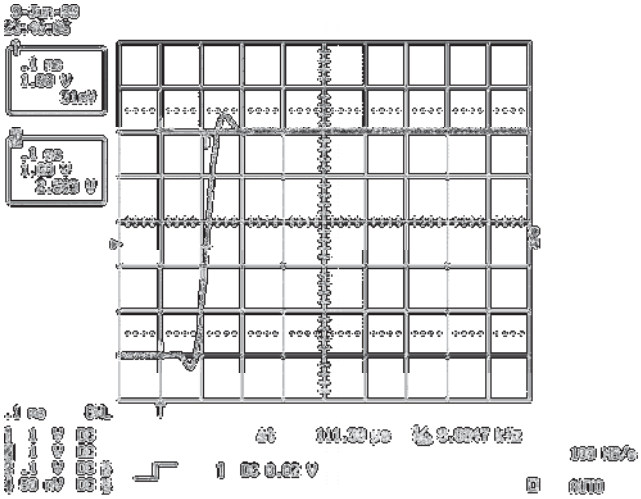


Figure 11-10: Hi-Speed Linear Phase, 10 kHz Corner, Narrowband

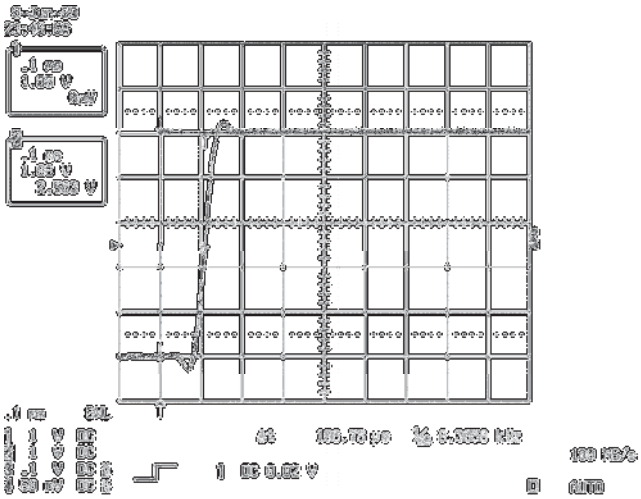


Figure 11-11: Hi-Speed Linear Phase, 10 kHz corner, Wideband

The Hi Speed Linear Phase filter is designed to operate at corner frequencies of up to 200KHz. The step response is nearly the same for both narrow and wideband modes.

12 Frequency Response

The frequency response data was obtained by measuring two sample filters. The data for each was plotted on the same chart. In most cases the data points were so close together that the plots look like a single line.

12.1 Frequency Response, Elliptic (Cauer)

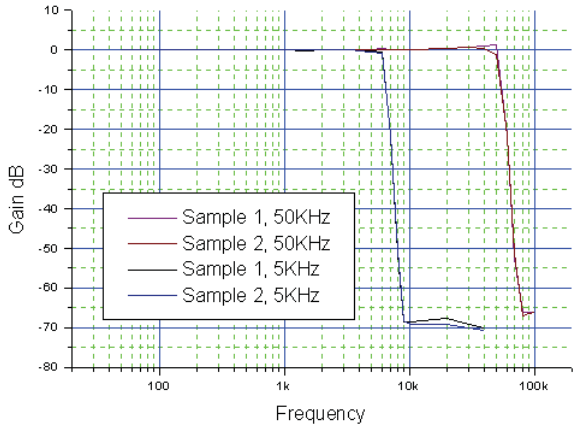


Figure 12-1: Elliptic (Cauer), Frequency Plot

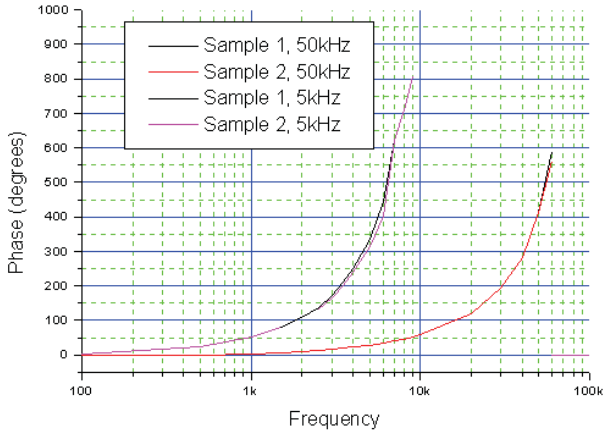


Figure 12-2: Elliptic (Cauer), Phase

12.2 Frequency Response, Butterworth

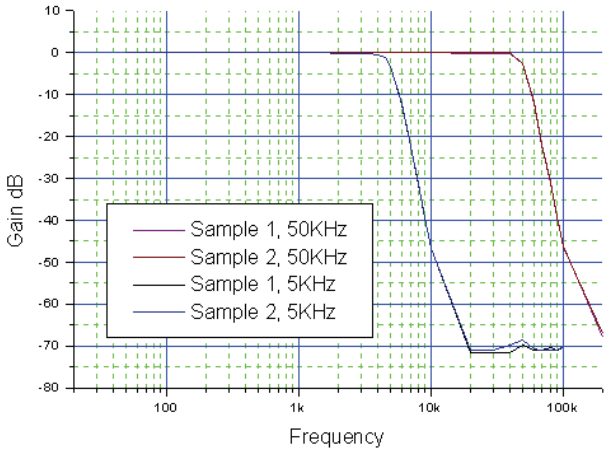


Figure 12-3: Butterworth, Frequency Plot

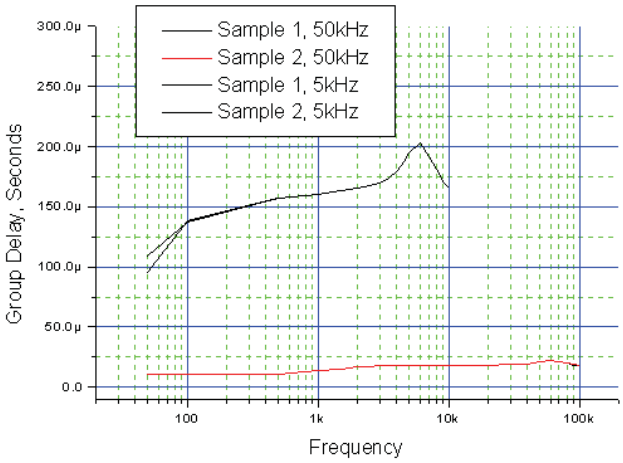


Figure 12-4: Butterworth, Group Delay

12.3 Frequency Response, Bessel

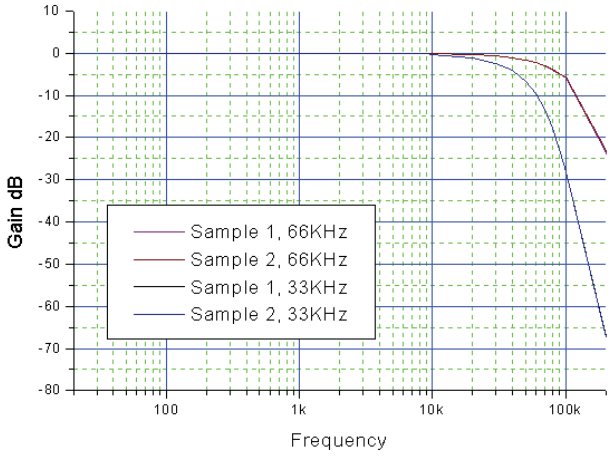


Figure 12-5: Bessel, Frequency Plot

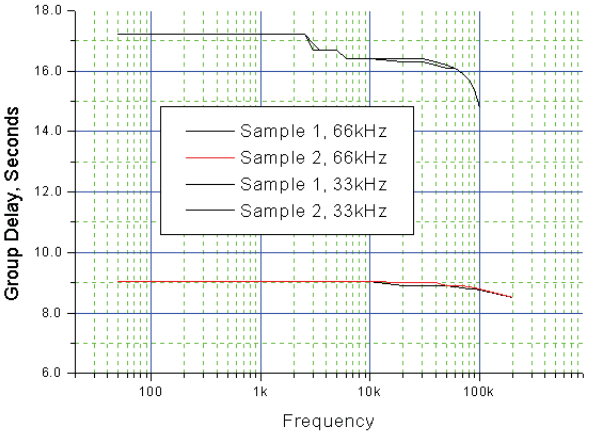


Figure 12-6: Bessel, Group Delay

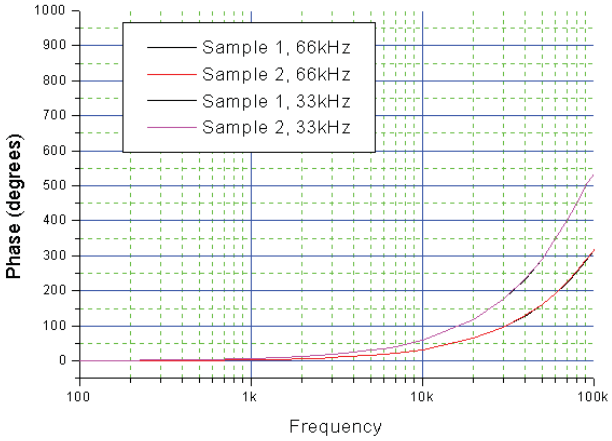


Figure 12-7: Bessel, Phase

12.4 Frequency Response, Hi-Speed Elliptic (Cauer)

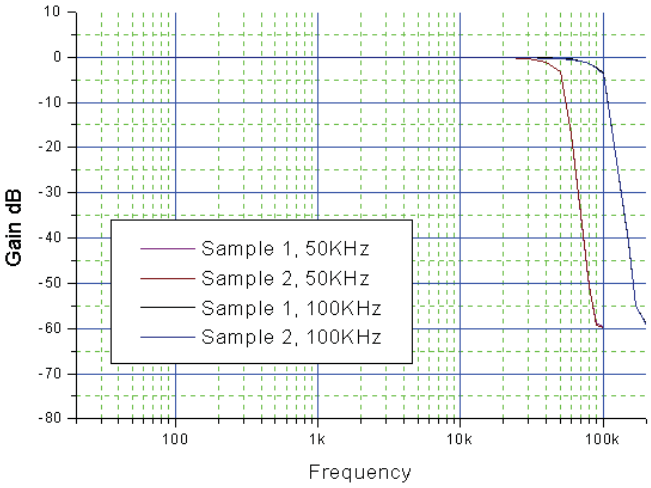


Figure 12-8: Hi-Speed Elliptic (Cauer), Frequency Plot

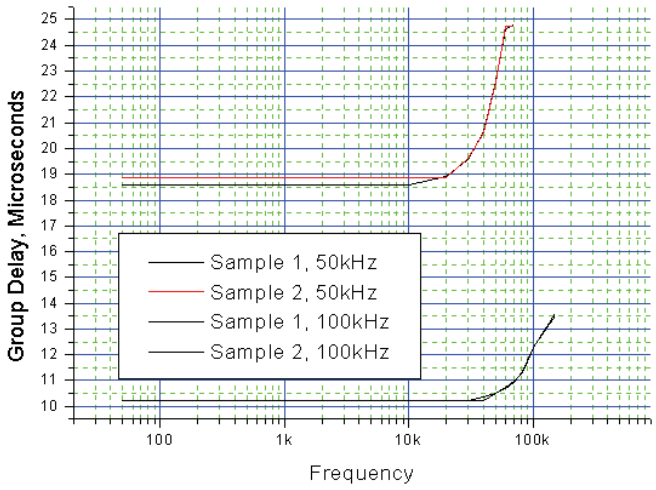


Figure 12-9: Hi-Speed Elliptic (Cauer), Group Delay

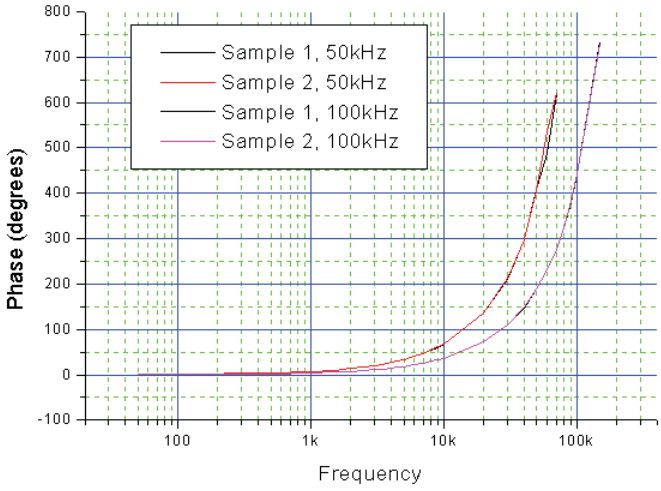


Figure 12-10: Hi-Speed Elliptic (Cauer), Phase

12.5 Frequency Response, Linear Phase

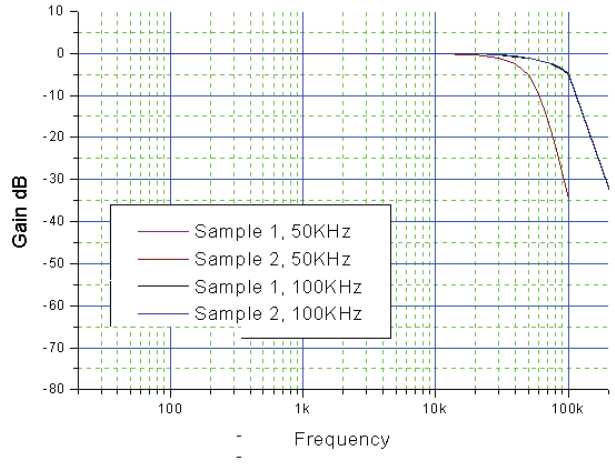


Figure 12-11: Linear Phase, Frequency Plot

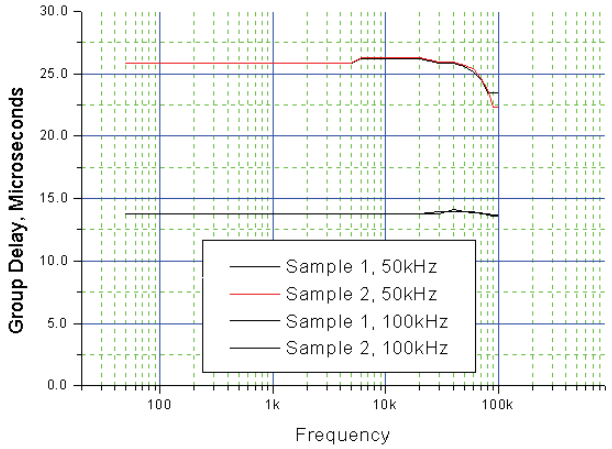


Figure 12-12: Linear Phase, Group Delay

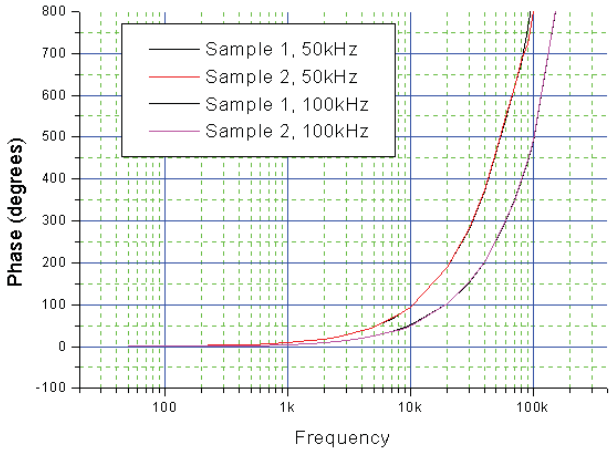


Figure 12-13: Linear Phase, Phase

12.6 Frequency Response, Hi-Speed Linear Phase

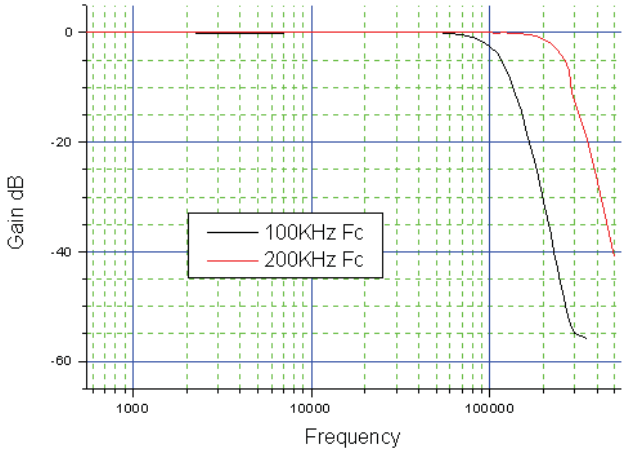


Figure 12-14: Hi-Speed Linear Phase, Frequency Plot

The frequency response for the filter is plotted for narrowband (Fc = 100KHz) and wideband (Fc = 200KHz).

The measurement equipment noise floor was approximately -70dB.

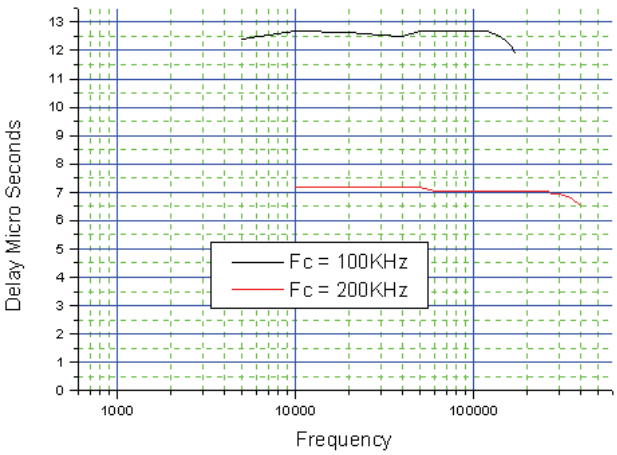


Figure 12-15: Hi-Speed Linear Phase, Group Delay

Group delay for the Hi-Speed Linear Phase filter is shown for both narrowband (Fc = 100KHz) and wideband (Fc = 200KHz) modes. Please refer to the data sheet for the Linear Technologies LTC1264-7, which is available at http://www.linear.com/prodinfo/ for further information on the group delay linearity of this filter.

13 USBPxxS1COM API for programming the USBPxx-S1 from custom software

To program the USBPxx-S1 modules directly from a custom software application, the ActiveX COM control, USBPxxS1COM.dll, must be loaded and initialized from the application program. Once initialized, the control can be queried to discover and connect the methods and events that define the interface to the control object. USBPxxS1COM.dll conforms to the COM standard and is registered with the operating system during the setup and installation process that loaded this documentation along with SystemViewUSBPxx on the target computer.

13.1 Distributing the custom software

To create the custom software distributable package, the following two controls must be installed and registered on the custom software target computer:

USBPxxS1COM.dll
HIDagentXControl1.ocx

These two files can be found in the subdirectory:

/program files/Alligator Technologies/USBPxxS1COM/distributable/

All standard install package creation software have options to register an installed component but if this must be done manually, there is a DOS (yes, DOS) command that can be used to do this. Open a DOS window to do this: Run CMD.

The DOS command is regsvr32. It is very simple to use. On each DOS command line type:

```
Regsvr32 USBPxxS1COM.dll
```

And then

```
Regsvr32 HIDagentXControl1.ocx
```

The best place to put these two files is in the \Windows\System32 area.

13.2 The COM Interface Initialization

An example custom software program is installed in the subdirectory:

/program files/Alligator Technologies/USBPxxS1COM/C++ ATL Example

The entire interface to USBPxxS1COM can be found in the file: TestClientDialog.h

The example was written in C++ using Microsoft Visual Studio 2010 C++ and utilizes the ATL framework included with the compiler. ATL, Active Template Library, is a complete set of code for creating COM objects but can also be used to create a COM client. A complete understanding of ATL is not necessary. ATL was used because it is convenient for illustrating the initialization steps necessary to load and initialize the USBPxxS1COM object. Every high level compiler or code generation tool that supports COM objects will follow the same steps used in this ATL based example to load and initialize the interface to the USBPxxS1COM object. There are 4 essential major steps:

1. The interface definition of the COM object must be loaded into the application. In the example, the line that does this is:

   ```
   #import "USBPxxS1COM.dll" no_namespace raw_interfaces_only
   raw_native_types named_guids
   ```

2. Define the event sink mapping where the COM control's events will be supported by the local event processing subroutines. The events will be individually documented in the next section. Defined here is the event linkage between the example application and the COM object event source. This is done with an ATL defined helper tool that defines the local event support mapping.

```
BEGIN_SINK_MAP(CTestClientDialog)
        SINK_ENTRY_EX(IDC_USBPxxS1CTL,DIID__IUSBPxxS1CtlEvents,1,DeviceConnected)
        SINK_ENTRY_EX(IDC_USBPxxS1CTL,DIID__IUSBPxxS1CtlEvents,2,DeviceDisconnected)
END_SINK_MAP()
```

3. An operating system call must be made to load the actual object into the application. In the example, an interface class variable was created using the ATL helper tool CComPtr. Passed to the ATL helper template is the interface name defined in the imported definition from step 1, IUSBPxxS1Ctl, that represents the COM interface definition class. The result is a pointer to the interface, pIUSBPxxS1Ctl.

   ```
   CComPtr<IUSBPxxS1Ctl>pIUSBPxxS1Ctl;

   hr = wndHID.QueryControl(&pIUSBPxxS1Ctl);
   ```

   The class wndHID, a class that we created in the example, was derived from the ATL library class that contains the method QueryControl. The interface pointer to the control is passed to QueryControl. There is a huge amount of abstraction in this subroutine call that makes life easy for us. QueryControl initializes the application linkage to the COM object and hooks up the event source to our event sink definition and makes the COM methods available to our application program. The variable, hr, is simply a status code that indicates whether QueryControl was successful or a failure occurred.

4. The final step is to call the USBPxxS1COM command method to initialize its own internal variables.

   ```
   pIUSBPxxS1Ctl->USBPxxS1Command(0,ID_INITIALIZE,0,0);
   ```

Once these 4 steps are complete, the events will fire when a powered USBPxx-S1 module is attached to or detached from the USB bus. More than one module can be attached to the USB bus simultaneously and each can be interfaced individually. USBPxxS1COM handles all of the complexities to establish an individualized communication link to each device. Each device is individually identified by a numeric ID called a handle. Use this handle to direct the USBPxxS1COM where to send information to or to query the information stored in each individual device.

13.3 The USBPxxS1COM Events

13.3.1 DeviceConnected Event

USBPxxS1 event handler DeviceConnected is executed when a USBPxx-S1 module is connected to the USB bus. The value Handle is passed by the operating system and is a unique identifier to be used in communication to the device. Common practice would be to read all of the previous values stored in the module and load up a data structure so that the application is aware of the current operation of the device.

13.3.1.1 Definition

void __stdcall DeviceConnected(long Handle)

13.3.1.2 Parameters

Handle – is a 4 byte long integer that represents the unique ID of the device connected.

13.3.2 DeviceDisconnected Event

USBPxxS1 event handler DeviceDisconnected is executed when a USBPxx-S1 module is removed from the USB bus. The value Handle is passed by the operating system and identifies which module was removed from the bus. Common practice would be to close all objects and variables related to the disconnected module.

13.3.2.1 Definition

void __stdcall DeviceDisconnected(long Handle)

13.3.2.2 Parameters

Handle – is a 4 byte long integer that represents the unique ID of the device connected.

13.4 The USBPxxS1COM Methods

There is one method for communicating to the USBPxxS1COM control. It is used to command the module to write a parameter to it or read a parameter from it. The command is a unique long integer value that defines which parameter is being passed. All data parameters passed in and passed out are 4 bytes in length. They can be integers, single precision floating point numbers, or characters, depending on the parameter to written or read.

13.4.1 USBPxxS1Command Method

13.4.1.1 Definition

```
HRESULT USBPxxS1Command (
                                LONG Handle,
                                LONG CmdID,
                                VARIANT* DataInPtr,
                                VARIANT* DataOutPtr);
```

13.4.1.1 Parameters

LONG Handle – a 4 byte long integer that represents the unique ID of the device connected

LONG CmdID – a 4 byte long integer. Parameters stored in the USBPxx-S1 can be read or written. This parameter identifies the parameter to be read or written. The values of CmdID are described in the next section in detail.

VARIANT *DataInPtr - The Variant data class is used in ActiveX COM controls where the data type is unkown at compile time. DataInPtr is defined as the address of the data. All data written to and read from the USBPxxS1 modules is 4 bytes long. Therefore single precision floating point numbers, the long data type, packed characters, and the revision code packed structure, can be transported across the USB link without the transport mechanism having to know the actual data type. Therefore the CmdID dictates the data type usage at both ends of the communication link. The DataInPtr points to data to be written to the device from the host. Some CmdID require input data defined and some do not. If DataIn is not required, then the pointer value should be NULL (0) or it simply can be defined and not used.

VARIANT *DataOutPtr - The DataOutPtr points to the address to recieve data from the device to the host. On commands to the host where data is written, the value can be used read error information from the device. The error codes are specific to the CmdID and discussed as needed in the sections below. On commands to the host where data is read, then this pointer should point to the repository for the read data.

13.4.1.2 Returns

HRESULT – long integer that is an operating system status that reflects whether the communication linkage to the COM object is working or not.

13.4.1.2.1 CmdID values

A C++ code example of each of the commands itemized below can be found in the example application. Look in the file: TestClientDialog.h

13.4.1.2.1.1 ID_INITIALIZE

Value = 0

Send this command first, before sending any other command. This will initialize all of the internal operation of the USBPxxS1COM.

13.4.1.2.1.2 ID_READ_LPFC

Value = 1

Read LPFc - LPFc is the low pass filter corner frequency and it is returned in OutVal.

InVal is not used.

OutVal = float LPFc

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.3 ID_READ_HPFC

Value = 2

Read HPFc - HPFc is the high pass filter corner frequency and it is returned in OutVal.

InVal is not used.

OutVal = float HPFc

Modules where this call is useful:

USBPHP-S1
USBPBP-S1

13.4.1.2.1.4 ID_READ_GAIN

Value = 3

Read Gain - Gain is the index value into a gain table and it is returned in OutVal.

InVal is not used.

OutVal = long Gain

Gain is an index into the following table:

0 = output signal is not amplified
1 = output signal is amplified 2x input signal
2 = output signal is amplified 5x input signal
3 = output signal is amplified 10x input signal
4 = output signal is amplified 20x input signal
5 = output signal is amplified 50x input signal
6 = output signal is amplified 100x input signal
7 = output signal is amplified 200x input signal
8 = output signal is amplified 500x input signal
9 = output signal is amplified 1000x input signal
10 = output signal is amplified 2000x input signal (Rev 5+ firmware)
11 = output signal is amplified 5000x input signal (Rev 5+ firmware)
12 = output signal is amplified 10000x input signal (Rev 5+ firmware)

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.5 ID_READ_COUPLING

Value = 4

Read Coupling – Coupling is an enable switch for DC or AC coupling the input signal to the module and it is returned in OutVal.

InVal is not used.

OutVal = long Coupling

0 = DC Coupling
1 = AC Coupling

Modules where this call is useful:

USBPGF-S1
USBPIA-S1

13.4.1.2.1.6 ID_READ_CLOCKSOURCE

Value = 5

Read ClockSource – ClockSource is a switch that determines the clock source for the low pass filter section. It can either originate from the internal clock generator controlled with the LPFc value or it can originate with an external clock source connected to the Ext Clk connection point and it is returned in OutVal.

InVal is not used.

OutVal = long Coupling

0 = Internal Clock
1 = External Clock

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.7 ID_READ_PCLOCK

Value = 6

Read PClock – PClock which is an abbreviation for Pacer Clock is a switch that determines if the internal clock source is output at the PClk pin and it is returned in OutVal. The Pacer Clock is useful when synchronizing an external data collection device to the internal clock generator.

InVal is not used.

OutVal = long PClock

0 = no output at PClk pin
1 = output enabled at PClk pin

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.8 ID_READ_CHANNELNUMBER

Value = 7

Read ChannelNumber – Channel Number is for informational purposes and it is returned in OutVal. The value can be set to any number and it does not affect the function of the module. It is usually used to inform operators of the data collection system, which input channel this module is physically connected to.

InVal is not used.

OutVal = long ChannelNumber

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.9 ID_READ_DESCRIPTION

Value = 8

Read Description – Description is a string of characters that can be used to provide labeling information to the operator. The command must be called repeatedly to retrieve a string of characters until an end of

string terminator is reached. Each character is packed into a 4 byte long space; The upper 2 bytes are used as an integer which represents the offset index into the string of characters, where 0 is the first character; The lower 2 bytes is used to hold a 1 or 2 byte character; The whole packet is returned in OutVal.

InVal is not used.

OutVal = structure {
Integer offset;
Integer Character;
};

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.10 ID_READ_LPFILTERTYPE

Value = 9

Read LPFilterType - LPFilterType is the low pass filter characteristic installed in the module and it is returned in OutVal. The value is an offset into an array of filter characteristics that are represented in the list below.

InVal is not used.

OutVal = long LPFilterType

0 = Cauer Elliptic 50kHz BW
1 = Cauer Elliptic 50kHz BW
2 = Bessel 33kHz BW
3 = Bessel 66kHz BW
4 = Butterworth 50kHz BW
5 = Butterworth 100kHz BW
6 = High Band Width Cauer Elliptic 50kHz BW
7 = High Band Width Cauer Elliptic 100kHz BW
8 = High Band Width Linear Phase 100kHz BW
9 = High Band Width Linear Phase 200kHz BW
10 = RESERVED
11 = RESERVED
12 = Linear Phase 50KHz BW
13 = Linear Phase 100KHz BW

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.11 ID_READ_HPFILTERTYPE

Value = 10

Read HPFilterType - HPFilterType is the high pass filter characteristic installed in the module and it is returned in OutVal. The value is an offset into an array of filter characteristics that are represented in the list below.

InVal is not used.

OutVal = long LPFilterType

0 = No High Pass Filter
1 = Bessel Normal Range
2 = Bessel Extended Range
3 = Butterworth Normal Range
4 = Butterworth Extended Range

Modules where this call is useful:

USBPHP-S1
USBPBP-S1

13.4.1.2.1.12 ID_READ_SERIALNUMBER

Value = 11

Read SerialNumber – The Serial Number is a manufacturing designation that facilitates quality control tracking and it is returned in OutVal.

InVal is not used.

OutVal = long SerialNumber

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.13 ID_READ_PRODUCTID

Value = 12

Read ProductID – The Product ID identifies what this module is and it is returned in OutVal.

InVal is not used.

OutVal = long ProductID

0 = USBPGF-S1
1 = USBPBP-S1
2 = USBPIA-S1
3 = USBPHP-S1

13.4.1.2.1.14 ID_READ_REVISION

Value = 13

Read Revision – The firmware revision code at manufacturing facilitates quality control tracking and it is returned in OutVal. It is to be used in the form X.Y where X is the major revision level of the firmware and Y is the minor revision level. Major is defined as a revision level in the public function interface. Minor is defined as a revision level in the private function areas.

InVal is not used.

OutVal = structure{
Integer MajorRevision
Integer MinorRevision
};

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.15 ID_WRITE_LPFC

Value = 14

Write LPFc - LPFc is the low pass filter corner frequency and it is placed in InVal. The status of the write operation is returned in the OutVal.

InVal = float LPFc

OutVal = status

0 = Successful
1 = LPFc out of range and not set

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.16 ID_WRITE_HPFC

Value = 15

Write HPFc - HPFc is the high pass filter corner frequency and it is placed in InVal. The status of the write operation is returned in the OutVal.

InVal = float HPFc

OutVal = long status

0 = Successful
2 = HPFc out of range and not set

Modules where this call is useful:

USBPHP-S1
USBPBP-S1

13.4.1.2.1.17 ID_WRITE_GAIN

Value = 16

Write Gain - Gain is the index value into a gain table and it is returned in OutVal.

InVal = long Gain

Gain is an index into the following table:

0 = output signal is not amplified
1 = output signal is amplified 2x input signal
2 = output signal is amplified 5x input signal
3 = output signal is amplified 10x input signal
4 = output signal is amplified 20x input signal
5 = output signal is amplified 50x input signal
6 = output signal is amplified 100x input signal
7 = output signal is amplified 200x input signal
8 = output signal is amplified 500x input signal
9 = output signal is amplified 1000x input signal
10 = output signal is amplified 2000x input signal (Rev 5+ firmware)
11 = output signal is amplified 5000x input signal (Rev 5+ firmware)
12 = output signal is amplified 10000x input signal (Rev 5+ firmware)

OutVal = long status

0 = Successful
3 = Gain out of range and not set

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.18 ID_WRITE_COUPLING

Value = 17

Write Coupling – Coupling is an enable switch for DC or AC coupling the input signal to the module and it is returned in OutVal.

InVal = long Coupling

0 = DC Coupling
1 = AC Coupling

OutVal = is not used. InVal is interpreted as bolean where only the lowest bit is used. It cannot be out of range.

Modules where this call is useful:

USBPGF-S1
USBPIA-S1

13.4.1.2.1.19 ID_WRITE_CLOCKSOURCE

Value = 18

Write ClockSource – ClockSource is a switch that determines the clock source for the low pass filter section. The clock can either originate from the internal clock generator controlled with the LPFc value or it can originate with an external clock source connected to the Ext Clk connection point and it is sent in InVal.

InVal = long Coupling

0 = Internal Clock
1 = External Clock

OutVal = is not used. InVal is interpreted as bolean where only the lowest bit is used. It cannot be out of range.

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.20 ID_WRITE_PCLOCK

Value = 19

Write PClock – PClock which is an abbreviation for Pacer Clock is a switch that determines if the internal clock source is output at the PClk pin and it is sent in InVal. The Pacer Clock is useful when synchronizing an external data collection device to the internal clock generator.

InVal = long PClock

0 = no output at PClk pin
1 = output enabled at PClk pin

OutVal = is not used. InVal is interpreted as bolean where only the lowest bit is used. It cannot be out of range.

Modules where this call is useful:

USBPGF-S1
USBPBP-S1

13.4.1.2.1.21 ID_WRITE_CHANNELNUMBER

Value = 20

Write ChannelNumber – Channel Number is for informational purposes and it is sent in InVal. The value can be set to any number and it does not affect the function of the module. It is usually used to inform operators of the data collection system, which input channel this module is physically connected to.

InVal = long ChannelNumber

OutVal is not used.

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

13.4.1.2.1.22 ID_WRITE_DESCRIPTION

Value = 21

Write Description – Description is a string of characters that can be used to provide labeling information to the operator. The command must be called repeatedly to send a string of characters. Send a 0 as an end of string terminator as the final character. Each character is packed into a 4 byte long space; The upper 2 bytes are used as an integer which represents the offset index into the string of characters, where 0 is the first character; The lower 2 bytes is used to hold a 1 or 2 byte character; The whole packet is sent in OutVal.

```
InVal = structure {
                Integer offset;
                Integer Character;
                };
```

OutVal is not used.

Modules where this call is useful:

USBPGF-S1
USBPBP-S1
USBPIA-S1
USBPHP-S1

14 Using the USBDR-8

The USBDR-8 is used to reduce the number of power cord and USB cables in a system. It can also be used to translate power voltage from high DC voltage sources to the low voltage requirements of the USBPxx-S1 units. External DC voltage input sources from 12V up to 50V can be used making the USBDR-8 an ideal power platform in trucks, boats, automobiles, and remote locations.

The USBDR-8 is designed to rest on a table top or it can be mounted directly to a wall. We also offer DIN rail mounting clips or can provide a 19" rack mount enclosure. In all cases the provided module hold down bracket should be used to lock the USBPxx-S1 units into the USBDR-8 connectors.

Each USBDR-8 has an uplink USB cable connector for connecting the USBDR-8 to a host computer and a down link connector for connecting to another USBDR-8's uplink connector. Up to 19 USBDR-8 can be linked together on the same USB uplink to the host computer.

There are no restrictions on the mixture of USBPxx-S1 types that can be used on the same rack. Since each unit is independent, a USBPGF-S1, USBPBP-S1, USBPHP-S1, and a USBPIA-S1 can reside on the same USBDR-8 and operate in unison.

When the USBDR-8 is fully populated with USBPxx-S1 units, it can get quite hot to the touch. This is normal and it is not overheating. The electronics will operate properly up to 80℃. Under normal conditions, the internal temperature of the center unit will reach 65℃. If the surrounding temperatur e is high and there is concern about overheating, set up a small DC powered fan to move the air past the USBDR-8.

14.1 USBDR-8 power connection

The USBDR-8 can be powered either from the supplied 24V 2A universal AC power adapter or from a DC source.

Figure 14-1 Powering the USBDR-8 from the supplied AC adapter

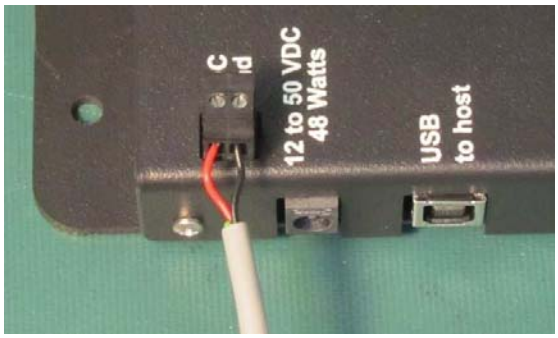


Figure 14-2 Powering the USBDR-8 from a DC source

14.2 USBDR-8 USB connection

Connect the USB to host connector to the host computer with the USB cable supplied. If multiple USBDR-8 are to be used on the same USB link, connect the USB down link connection to the next USB to host uplink connection and so on. Up to 19 USBDR-8 can be connected on the same USB uplink to the host computer.

14.3 USBDR-8 hold down bracket

The supplied hold down bracket for the USBDR-8 should be used to keep the USBPxx-S1 units securely connected to the USBDR-8 connectors. If the bracket is not used, an intermittent connection can occur between the USBDR-8 and the unit and this can interfere with signal throughput or USB communication control. The hold down bracket can be used with an number of USBPxx-S1 units installed.

Figure 14-3 A fully populated USBDR-8 with hold down bracket in place

Figure 14-4 Use the supplied washer and screws to securely fasten the hold down bracket to the USBDR-8

14.4 USBDR-8 external clock control

In applications that require multiple filters tracked to the same corner frequency, the filter clocks of each module can be tied together. Use the External Clocks header for this purpose. If one unit is to control all of the other units, then in software set the control unit to Pacer Clock enable output and set the other units to an External Clock Source.

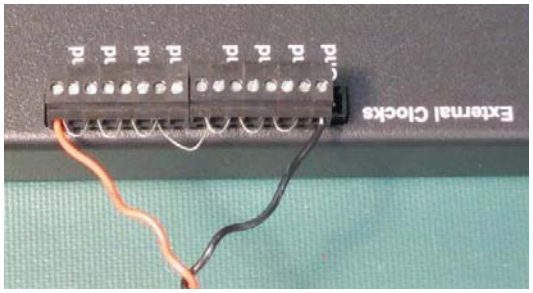
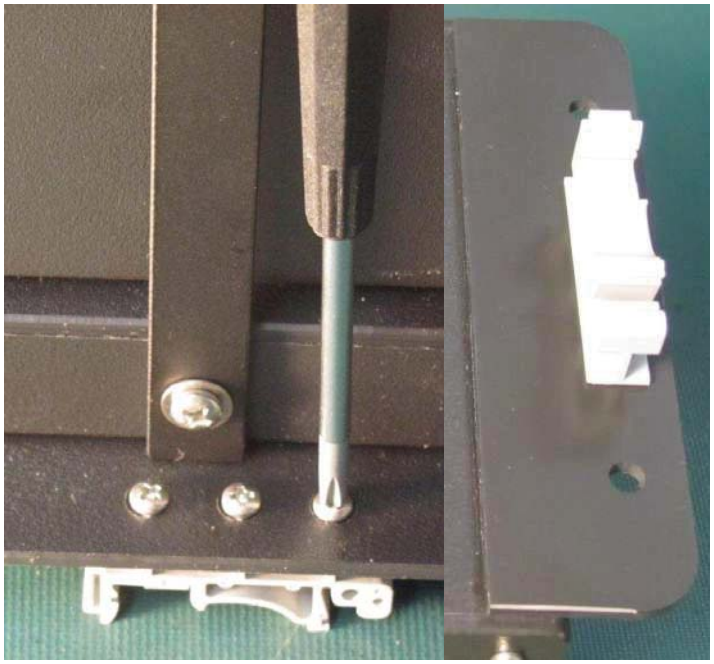


Figure 14-5 Pictured is an 8-channel synchronized connection to an external clock source

14.5 USBDR-8 DIN rail clips

The USBDR-8 can be clipped to a DIN rail. The DIN rail mount kit can be purchased as an accessory. Please refer to the USBDR-8/DRM part number in our price list.



14.6 USBDR-8 19” rack mount enclosure

The USBDR-8/RMK is an optional 19” rack mount assembly for the USBDR-8. We recommend using the hold down bracket in addition to the face plate when securing the USBDR-8 and the USBPxx-S1 units to the rack mount assembly. Assemble the USBDR-8 first and then mount the completed assembly using the supplied USBDR-8 mounting bolts.

Orient the side cutouts on the rack mount assembly with the USB and power connectors on the USBDR-8.

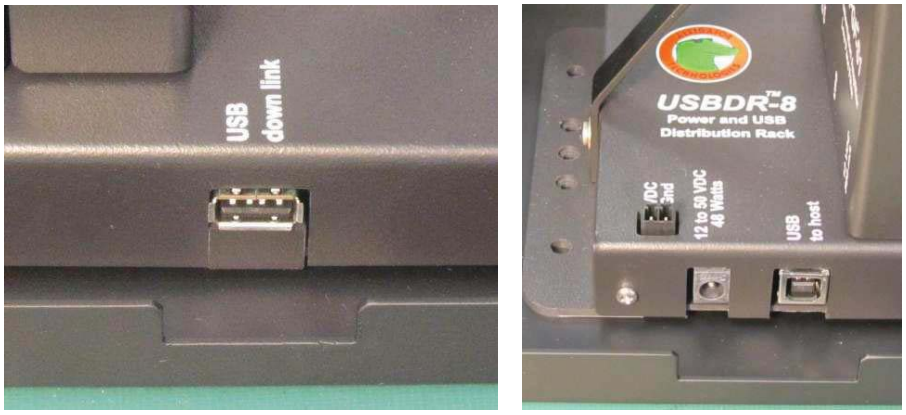


Figure 14-6 Orient the rack mount enclosure cutouts with the USBDR-8 connectors

Figure 14-7 Use the supplied USBDR-8 mounting bolts and washers to secure the USBDR-8 to the rack mount enclosure

Figure 14-8 first secure the base assembly to the rack with the inset rack bolts and then secure the face plate to the rack mount assembly with the supplied rack bolts and plastic washers.

References

Many good references exist. The favorites, in no particular order, at Alligator Technologies are:

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